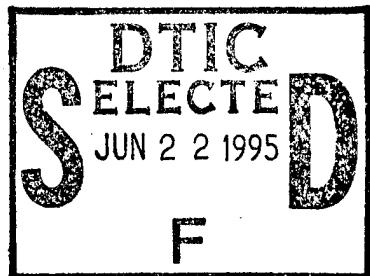


NAVAL POSTGRADUATE SCHOOL

Monterey, California



THESIS

TESTING OF A CMOS VLSI IC FOR REAL-TIME OPTO-ELECTRONIC TWO-DIMENSIONAL HISTOGRAM GENERATION

by

Peter J. Reinagel

March 1995

Thesis Co-Advisors:

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TWO-DIMENSIONAL HISTOGRAM GENERATION**

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Lieutenant, United States Navy
B.S. Computer Science, University of South Carolina, 1989

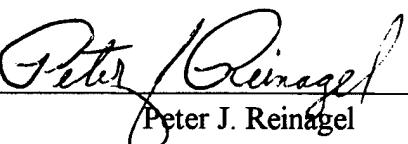
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of the requirements for the degree of

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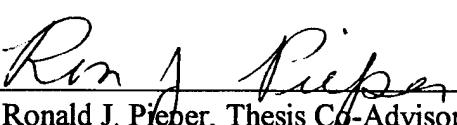
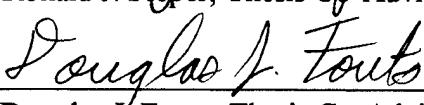
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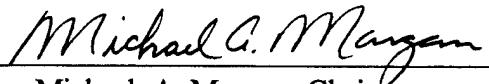
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ABSTRACT

A recently fabricated CMOS VLSI IC was designed to generate two-dimensional histograms in real-time on digital computers. This thesis reports the efforts to determine if the 2DHIST IC chip functions as designed. Tests were conducted with a logic analyzer, general purpose electronic test equipment, and circuit simulation software.

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I. INTRODUCTION

A. BACKGROUND

Histograms are useful for graphically representing data over a range of frequencies and indicating by height, the number of frequencies occurring within that range. A histogram generated in real-time provides a type of data reduction which enables critical decisions to be made with greater ease than by examining raw data. To cite one industrial example, the forest products industry would like to know before sawing a valuable hardwood log if it is of suitable quality to veneer it or if it should be made into lumber. They can now use histograms to present the results of an x-ray computed tomography (CT) scan of the hardwood logs. In this process, hundreds of CT images are filtered and presented as histograms representing internal defects within the log. Knowing the severity and location of defects within a log allows the decision maker to make an educated decision to veneer or cut the log for lumber. The histogram data applied here aids in making a costly decision where there could be a factor of 10 difference in value for the two products. [Ref. 1] Similarly, the medical field, attempting to locate tumors could utilize histograms to present the results of CT scans. Material inspection systems and process monitoring are two disciplines that could readily use an IC chip that performs histogram generation in real-time.

For operations which demand real-time signal processing, it is documented that the Fourier Transform [Ref. 2] and the Hough Transform [Ref. 3] are too computationally intensive to be done in real-time on digital computers. Duncan, Poon and Pieper [Ref. 4] have developed an edge-extraction technique for binary images which uses a technically simple optical-electronic system. This project has evolved into an alternate method of producing real-time histograms on a digital computer by processing optical inputs in a mixed signal analog/digital circuit. It is the realization of this work in the form of a 2μ CMOS VLSI IC chip that is the object of this research.

B. RESEARCH GOALS

The first prototype is a one-dimensional histogram generator referred to as 1DHIST and the second version is a two-dimensional histogram generator referred to hereafter as the 2DHIST. The 2DHIST IC chip was conceived to take advantage of the miniaturization possible with VLSI techniques for the timing and histogram generation circuits. A tradeoff was made to fabricate the 2DHIST in a 2μ CMOS process versus the 0.5μ technology available today strictly for the savings in cost. If the chip can demonstrate functionality, then it would have validated the two-dimensional histogram generation concept at 2μ while conserving the limited fiscal resources available to the NPS as a government educational institution. MOSIS, the semiconductor brokerage organization, with funds received from the National Science Foundation, arranged for fabrication of the 2DHIST. Twelve chips mounted in 65 lead pin grid array (PGA) packages were received from the run. The chip dimensions are 6.5 mm x 3.7 mm.

The purpose of this research was to determine if the recently fabricated real-time opto-electronic two-dimensional CMOS VLSI histogram generator IC chip [Ref. 5] functioned as designed. To make this determination and to quantify performance, a test bed was wire wrapped and a series of tests were run on the 2DHIST chips. Then, data comparison and analysis was done between the prefabrication simulation data and the test results gathered on the actual 2DHIST chips.

C. THESIS OUTLINE

This thesis is divided into three main sections. The first discusses the need for a two dimensional histogram generator and describes the theory of operation. The second section covers the computer simulations and testing on the recently fabricated 2DHIST IC chips. The final section describes the test results and further research for two dimensional histogram generation utilizing a 2μ CMOS P-well process.

The emphasis of this work has been on testing but test results are certainly more meaningful when the theory of operations are understood. In Chapter II, the theory of the 2DHIST IC chip operation is briefly explained.

The 2DHIST chip testing is discussed in Chapter III. Details of the test configuration and procedures are given. An explanation of the HP Logic Analyzer System and how it was used to stimulate and record outputs of the 2DHIST is provided. This chapter also describes the software tools used in the layout and simulation of the architecture. Included are screen captures of the resulting waveforms and listings of the test vectors. The expected test results and the rationale for such are explained. Actual test results are documented and contrasted with the expected results.

The next chapter explains the computer simulation done in Pspice, a commercial circuit analysis software program. This mixed mode simulation of the 1DHIST system served as a concept validation for the 2DHIST. The 1DHIST system was previously built and tested in the laboratory at Virginia Polytechnic Institute and State University [Ref. 4].

In Chapter V, the actual test results are summarized and analyzed. Theories on why some 2DHIST chips performed less than ideally are offered. This final chapter draws some conclusions and suggests areas for further research.

II. TWO-DIMENSIONAL HISTOGRAM GENERATOR

OPERATION

The 2DHIST is relatively straightforward, both in overall purpose and in the circuit layout. The designer [Ref. 5] intended this IC to implement the digital portion of a system that will be used to produce waveforms on an oscilloscope in a mathematical histogram pattern, based on the amount of light passing the object being examined. The unique terms used are defined before a full explanation of the theory of operation is provided.

A. TERMINOLOGY

For the sake of clarity, definitions are given for those signals terms that may not be familiar or that could possibly be ambiguous.

- ◆ CAD, Computer Aided Design.
- ◆ CIF, Caltech Intermediate Format. A layout description language to transfer mask level layouts [Ref. 6].
- ◆ CMOS - complimentary metal oxide silicon .
- ◆ ESD, Electrostatic Discharge.
- ◆ ESIM, Event Simulator.
- ◆ FSM, Finite State Machine.
- ◆ GUI, Graphical User Interface.
- ◆ MC - master clock, a timing pulse used for sequencing events in the histogram generation circuit.
- ◆ PC - pulse clock, a timing pulse used to control the mirror.
- ◆ SC - scan clock, a timing pulse used to control the sampling of input.
- ◆ PGA, pin grid array.
- ◆ one-shot, is also known as a retriggerable monostable multivibrator and is a circuit that emits a pulse at a set rate. For the 2DHIST, this pulse is a function of MC and has a width of about 3 ns.

- ♦ MOSIS - metal oxide semiconductor integration service. This microelectronics brokerage service is provided by the Information Sciences Institute of the University of Southern California. MOSIS is a low-cost prototyping and small volume production service for custom VLSI circuit development. They are able to charge minimal fees because they aggregate designs from various educational institutions, DoD, and commercial companies onto a single mask set. This allows the chip designers to share fabrication costs. MOSIS subcontracts for the actual fabrication to industry IC chip foundries.
- ♦ VLSI - very large scale integrated. A style of circuit design that typically has many thousands to over one million components incorporated into a single chip.
- ♦ ZIF, Zero Insertion Force.

B. THEORY OF OPERATION

To better understand the theory of operation, the reader is encouraged to refer to Figures 1 and 2. Figure 1 depicts the overall system to be ultimately built. The narrow laser beam is reflected off the mirror and through lens, L1. The mirror controller repositions the mirror to allow scanning the light beam over the surface of an object in a raster pattern. The light beam next hits the object of interest and a portion of light this will continue onto lens, L2. Lens, L2 will collimate a beam on the photodetector. The photodetector circuit will generate an analog voltage proportional to the amount of light detected. This analog signal is input to the histogram generation circuit. This logic, with controlling inputs from the timing circuit, produces a proportional histogram-style waveform on the oscilloscope. The clock pulse generation circuit produces three pulses: MC, PC and SC and these are used by the timing circuit to synchronize mirror movement with the logic and the oscilloscope.

In the 2DHIST system, there are some key differences from the original system. In the 2DHIST system, only MC and SC are required as inputs to the timing circuit. This is because in the 2DHIST the timing circuit is implemented as a finite state machine (FSM). However, the PC signal is still used to control the mirror. A second mirror would be

required to realize the second dimension while doing a raster scan of the object. Richstein, Fouts and Pieper [Ref. 7] capitalized on the benefits of VLSI and built an IC chip which incorporated the majority of the histogram generation circuit and all of the timing circuit. The design and layout of the 2DHIST timing and histogram circuits are presented in detail in Richstein's thesis. [Ref. 5] The histogram generation circuit merits further explanation because it is the key element of the system.

Figure 2 is a block diagram of the functional blocks of the histogram generation circuit. Although the function of this circuit is the same for both the 1DHIST and the 2DHIST, the accuracy, speed, and implementation differ. First, a description of how the 1DHIST works is presented and then a discussion of the changes made in the 2DHIST follows.

The input that drives the histogram generator is the photodetector signal, an analog voltage. The peak detectors save the maximum and minimum photodetector signals sensed as V_{ref+} and V_{ref-} . The resistor ladder then determines the voltage boundaries for electronic bins based on the dynamic range of the peak detector signals. This is not unlike dividing the frequency spectrum into bands. The comparator bank is comprised of operational amplifiers. The comparator bank compares the output of the resistor ladder with the buffered signal from the photodetector. The state of the comparator bank, a sequence of high and low voltage levels, determines into which electronic bin the photodetector's signal will go. Next the comparators' analog high or low voltage output is converted to transistor-to-transistor logic (TTL) levels so that signals will be compatible with the digital circuitry which follows. The next portion of the circuit is digital logic.

Using timing signals, the sampling bank gates either a logic one or a logic zero to the counters. A one-shot is used to sample at regular intervals; 75 ns for the 1DHIST and 3 ns for the 2DHIST. A logic one going into a particular electronic bin represents the photodetector signal at a specific moment in time. The sampling bank is simply exclusive-or (XOR) and AND logic gates. The sampling ensures that the digital count in

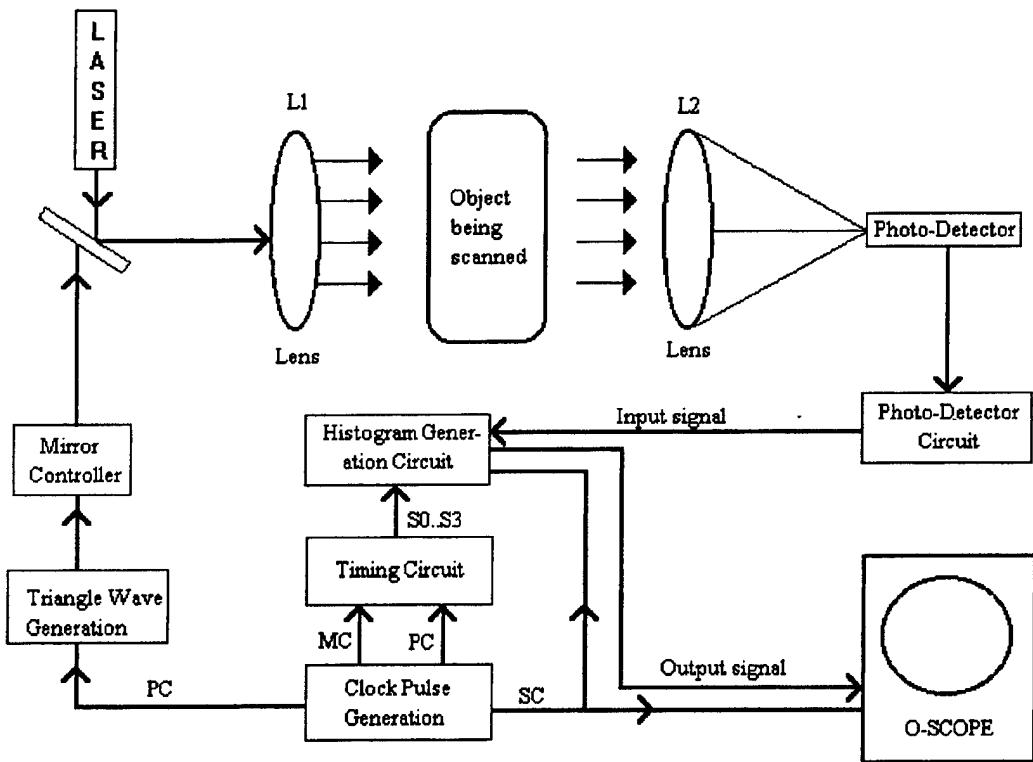


Figure 1. After Ref. [5]. 1DHIST System Design

the electronic bin corresponds to the amount of the photodetector signal that belongs in that bin. Therefore, the count in the counter bank is indicative of the amount of light that was incident on the photodetector at a given time in the scan cycle. Eight bit binary counters constitute the counter bank in the 1DHIST. The multiplexers are used to sequentially gate out the count data so a histogram can be constructed. Additional timing signals and outputs from the finite state machine control the multiplexers. Beginning with the lowest voltage, the multiplexer digital output is converted back to an analog voltage by another resistor ladder for presentation on an oscilloscope as a histogram. [Ref. 8]

In the 2DHIST, the sampling bank, the sampling pulse (from a one-shot device), the counters, the multiplexers, and the timing circuits are implemented in CMOS VLSI. An external clock is required to produce the master clock, pulse clock, and scan clock

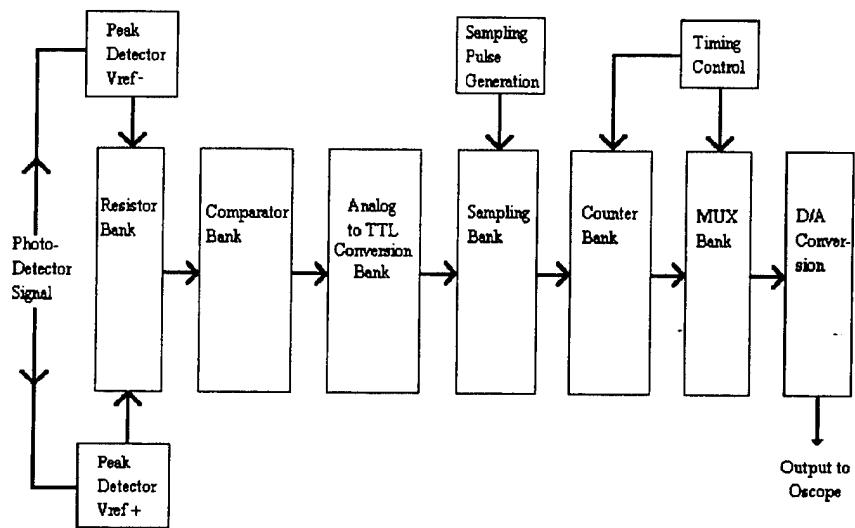


Figure 2. After Ref. [5]. Histogram Generation and Timing Circuits

signals. The MC is higher than the PC by a factor of 32 and it is a factor of 64 higher than the SC. We have used a MC of 1 MHz down to approximately 1 KHz in the lab and in simulations.

III. IC TESTING

MOSIS, the microelectronics brokerage service delivered 12 2DHIST ICs to the NPS. The goal of the research was to determine the functionality of these ICs and to quantify their performance.

A. TEST BENCH SETUP

The requirements for the test bench were that it should be capable of supplying all input signals to the 2DHIST chip and monitoring the data outputs. This meant having a power supply, signal generation equipment, data monitoring and recording devices. Figure 3 illustrates the specialized and general purpose electronic test equipment used to test the 2DHIST chip. After the 2DHIST layout was sent for fabrication, a logic analyzer was acquired to facilitate testing of this IC and other VLSI ICs. Several vendors' product lines were reviewed and ultimately the Hewlett Packard HP16500B Logic Analysis System was purchased.

It may not be apparent why a logic analyzer was chosen over the more common and familiar oscilloscope. This is because a logic analyzer allows many signals to be seen at once instead of the few an oscilloscope can display. Also, a logic analyzer shows the signals in the system in the same way that they appear to the hardware under test. The increased number of data signals being monitored comes at the expense of resolution. [Ref. 9] This tradeoff was acceptable for testing the 2DHIST ICs.

1. HP16500B Logic Analysis System

The advantage to using the HP16500B is that it combines a pattern generator and a logic analyzer in one instrument. The pattern generator produces waveforms that are used to stimulate the IC chip under test when the appropriate ribbon cables, called pods by Hewlett Packard, and test leads are connected. For testing the 2DHIST ICs, CMOS Tri-State Buffers were attached to the signal pods from the pattern generator to assure proper voltage levels going to the chips. Since the 2DHIST chip does not utilize tri-state logic, the tri-state pin was connected to ground. Then, with the proper test leads, the outputs of the IC being tested were input to the logic analyzer. Here the signals may be

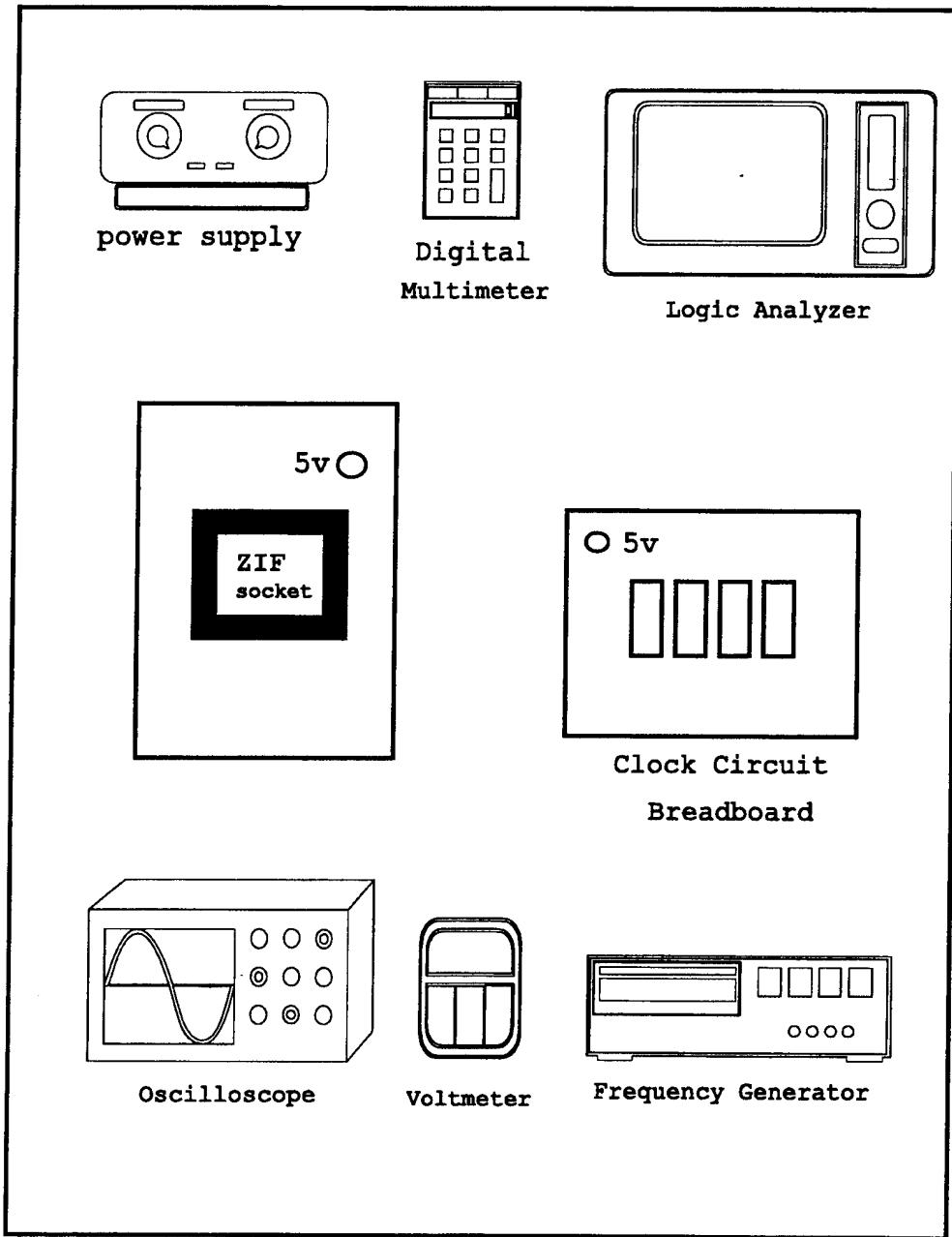


Figure 3. Test Bench

displayed on the built-in cathode ray tube (CRT) and stored on the internal 80 Mb hard disk drive or to a removable 3.5" diskette. Menu options indicate data can be sent directly to a printer via an RS 232C port. However, in our experience, this was not possible despite various configurations and numerous attempts. This caused minor difficulty when extracting data from the HP16500B. The HP16500B is controlled by a graphical user interface (GUI) making it user friendly. The operator has the option of using the touch screen menus or the mouse to input menu selections. There is no keyboard on this model.

a. Pattern Generator

The pattern generator has the ability to execute a single list of instructions or macros. These macros are short programs designed to simplify the coding of test routines. More importantly, these macros permit code to be written once and used repeatedly. Macros on the HP16500B are not in a specific programming language. However, they are written in such a high level language that the macro consisted of almost plain English statements. The program written to test the 2DHIST was merely to send a string of ones and zeros to the IC chip as shown in Figure 4. Eventually, more elaborate macros would be required to adequately simulate the full range of signals possible from a photodetector in a system as described earlier.

b. Logic Analyzer

The logic analyzer was configured to receive digital data pulses from the 16 multiplexer output pins of the 2DHIST. Additionally, control signals which were produced by the 2DHIST chip were monitored by the logic analyzer. This was possible because the designer brought each signal made on chip to a separate output pin. This provided great flexibility in testing. For example, with three one-shot outputs to choose from, the tester can select which one will be connected to the one-shot input pin. In fact, these output signals must be connected with wire wrap or jumpers to the corresponding input pin for the 2DHIST chip to function.

PATTERN GENERATOR PROGRAM LISTING

Instruction	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
	Binary							
SIGNAL IMB	0	0	0	0	0	0	0	0
ZEROS	0	0	0	0	0	0	0	0
PARAMETERS	0	0	0	0	0	0	0	0
ONES	1	1	1	1	1	1	1	1
PARAMETERS	1	1	1	1	1	1	1	1
BREAK	0	0	0	0	0	0	0	0

PATTERN GENERATOR MACRO 1 LISTING

Instruction	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
	Binary							
ZEROS	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
PARAMETERS	PARAM2							
REPEAT 16	0	0	0	0	0	0	0	0

PATTERN GENERATOR MACRO 2 LISTING

Instruction	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
	Binary							
ONES	IN0	IN1	IN2	IN3	IN4	IN5	IN6	IN7
PARAMETERS	PARAM2							
REPEAT 16	1	1	1	1	1	1	1	1
BREAK	1	1	1	1	1	1	1	1

Figure 4. Test Program for 2DHIST Chip

The data was displayed as positive logic digital signals (i.e., a high level or logical one is shown as the raised portion of the waveform). The logic analyzer was synchronized with the histogram generation circuit by feeding the externally generated clock signals, MC and SC into the logic analyzer. Pod 5, pin N had the master clock, MC, and pod 6, pin P, had the scan clock, SC.

2. Testbed

The IC under test needs to be mounted securely so that there are sound electrical connections on all signal pins. It was decided to mount the 2DHIST chip in a 13 by 13 PGA zero insertion force (ZIF) socket to allow very simple swapping of chips. Since the ZIF socket has only very short pins, it was mated with in-line wire wrap sockets. The leads from these wire wrap sockets were inserted into a perforated board. These leads were of sufficient length to hold wire wrapped jumper lines or to attach the signal lines from the Logic Analyzer System. The ZIF socket, perforated board, and the associated connections are collectively referred to as the testbed.

Appendix B contains the pinout for the 2DHIST chip and all the details on where to install the jumpers necessary to test it. Figure 5 shows the numbering of the pins on the 2DHIST package. Pins are referenced as an alphanumeric pair (i.e., pin B9 = 48). This is the view from the top of the PGA (i.e., no pins are visible).

3. General Purpose Test Equipment

To properly test the 2DHIST chips, various pieces of common test equipment were required. Table 1 lists the general purpose test equipment used.

4. Clock Circuit

The 2DHIST IC chip requires two square wave clock signals as inputs. These signals are MC and SC which are used to sequence events. These signals were also fed into the logic analyzer to synchronize it as mentioned above. Four 74LS193 IC chips were cascaded to produce the master clock at 976.56250 Hz and the scan clock at approximately 15.25878 Hz. The relationship between these apparently peculiar frequencies is that they are in phase and are derived from a 1 MHz input. The Wavetek

K	J	H	G	F	E	D	C	B	A	
17	15	13	11	9	7	6	4	3	1	1
19	16	14	12	10	8	5	2	64	63	2
20	18					65	62	61		3
22	21						60	59		4
23	24						58	57		5
25	26						56	55		6
27	28						53	54		7
29	30						50	52		8
31	32	34	37	40	42	44	46	48	51	9
33	35	36	38	39	41	43	45	47	49	10

Figure 5. Pad to Pin Layout, Top View

DESCRIPTION	MAKER	MODEL	SETTINGS
DC Power Supply	BK Precision	1646	5 Volts, current switch low
Oscilloscope	Hewlett Packard	HP 1741A	DC coupling, chop, trigger: CH B, main trigger: LF REJ, display: main
Frequency Generator	Wavetek	142	1 MHz square wave, + DC offset, 0 dB output attenuation
Digital Multimeter	Hewlett Packard	HP 3466A	various
Voltmeter	John Fluke	27	various

Table 1. General Purpose Test Equipment

frequency generator supplies this signal to the clock circuit. A coaxial cable was used between the frequency generator and the clock circuit breadboard to reduce noise on the clock signal. The $50\ \Omega$ output of the Wavetek was connected to pin 5 of the first of four 74LS193 IC chips in the clock circuit.

The 74LS193 ICs are designed as four-bit programmable synchronous up/down counters. They were configured as up counters. The clear function was not used but the clear line, pin 14, was required to be held low on the National Semiconductor chip set used. The MC signal is tapped off of pin 2 on the third 74LS193 chip and the SC signal is from pin 7 on the fourth 74LS193 chip. Figure 6 shows the clock circuit.

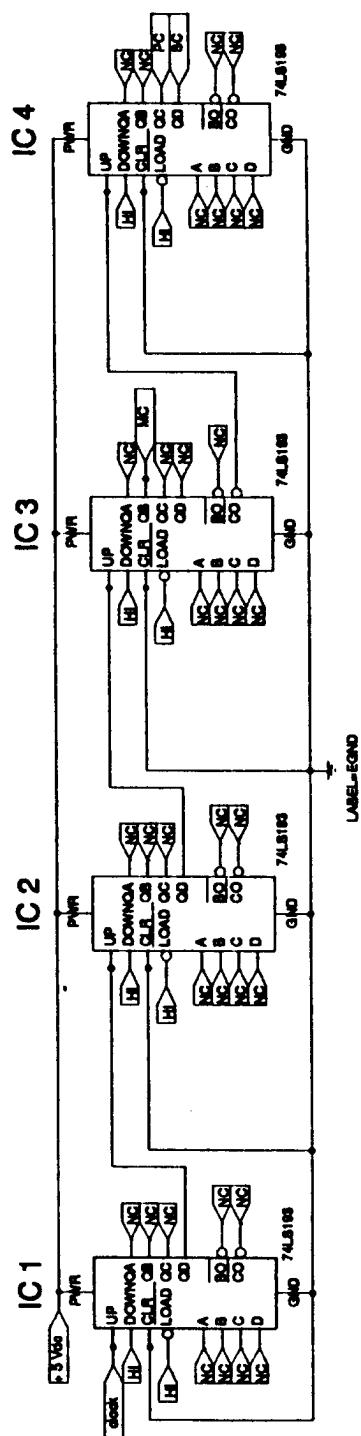
It is worth noting that the HP16500B Logic Analyzer System was not able to generate clock signals that met our requirements. The HP16500B allows a user to program up to three clock signals which can be used externally via the strobe pins on pod B3. However, the system only permits a single period for all three of the clock signals and further limits the user to a selection of just 13 predetermined periods. These range from 20 ns to 200 μ s. Since the periods of the MC and SC signals are almost an order of magnitude apart, it is not possible to define them on the HP16500B.

This significant difference between the clock periods also made it more challenging to observe both MC and SC on the oscilloscope simultaneously. With patience and the proper adjusting of the delay dial, we observed MC and SC together on the HP1741A oscilloscope and confirmed the 74LS193 clock circuit produced in-phase clock pulses.

B. TESTS CONDUCTED ON THE 2DHIST CHIP

Various tests were run on the 2DHIST chip set to ascertain their operability. These tests and verifications include:

1. Continuity checks
2. HP Pattern Generator Tests
3. Event Simulation (ESIM) on the FSM
4. Latchup Test
5. Magic layout verification



Note: Signal on the UP pin of IC 1 is a 1 MHz square wave from the Wavetek Frequency Generator.

Figure 6. Clock Generation Circuit

6. Visual trace using the MicroManipulator

Only tests one and two were part of the initial test plan. When the data on the first two chips did not match pre-fabrication simulations or yield the desired outputs, tests three through six were added. Before describing the actual testing, a brief note about test practices. At all times there was a concern about electrostatic discharge (ESD) when handling the IC chips. The workbench has an ESD mat covering it and a conscious effort was made to discharge static electricity prior to handling any IC chip. When 2DHIST IC chips were not in the ZIF socket, they were pressed into a low-density rubber foam and kept in a jewel case. There is no reason to believe any ESD damage occurred.

1. Continuity Checks

Using the HP3466A Digital Multimeter, continuity was checked between many pairs of pins. Initially, checks were made for any clear problem signs, such as power and ground pins indicating a short and none were found. All power pins for the guard ring and the chip (C2, F9, G1, J2) were connected together. The ground pins for the guard ring (C10, K10) and the chip (E10, G2) had a short between the respective pairs. No unexpected shorts or opens were found on the various chips checked.

In this process, an "extra" pin was discovered. That pin being pin C3. Here "extra" means that only 64 pins were in the layout file sent to MOSIS for fabrication and yet the IC chips shipped have 65 pins. Appendix B has more discussion on this pin.

2. HP Pattern Generator Tests

The HP16500B Logic Analyzer System was the cornerstone of our testing efforts. The pattern generator was programmed to stimulate the 2DHIST IC chips with contrived data strings to emulate live data from a photodetector. The operator has great flexibility in programming the pattern generator. A list of signals are entered as labels and pin assignments to individual lines in the pods are made. For all these tests, signals were coded as binary; either a logic one or zero.

It is also necessary to set the trigger levels on the HP16500B. The trigger is used to determine on which signal level to begin sampling. This is done by clicking the mouse

on the trigger icon and setting trigger values. Trigger values can be set to logic one, zero or "x", the "don't care" state. For these tests the trigger term, "a" was used and all signals were set to trigger on "x". Refer to Figure 7 to see a sample of trigger settings that are representative of all trigger values.

The expected results from the 2DHIST chips are as follows. The data lines shown should have had a pattern of logical ones and zeros corresponding to the pattern in the macro. The one-shots should have 3 ns width pulses. The state lines, S0 through S3, should behave like a divide-by-N circuit. S0 should change half as often as MC and S1 should toggle half again as much as S0, or one quarter the frequency of MC. State S2 is half the frequency of S1 and S3 is half of S2's frequency. The control signals, clear and muxen should toggle and not be constant.

After getting no pulse on virtually all signal lines from the finite state machine and the one-shots, control signals from the pattern generator were substituted to eliminate the FSM and one-shots as sources of problems. This was to no avail. Figures 8 and 9 show typical waveforms from the logic analyzer. The waveforms in Figure 8 monitor activity on 14 of the 16 multiplexer outputs. Output pins OO and OP were omitted because of space limitations but they behaved the same as the other data lines. The other eight control signals from the FSM or one-shots were likewise without signs of activity. Figure 9 tells a similar story but here less lines are displayed for ease of interpretation. To rule out possible loading effects, the outputs of the FSM were disconnected from the multiplexers and only went into the logic analyzer for monitoring. This isolation did not change the output signal levels. There were numerous changes to the configuration of the pattern generator and the logic analyzer in the hopes that the lack of valid signal output from the first two 2DHIST chips was due to improper setup. In fact, the setup of the HP16500B was questioned frequently because the operator had no previous experience with logic analyzers and only one other student has tested an IC chip on it here.

Eventually, a decision was made to test the entire chip set to determine if the entire batch was defective. The risk that the HP16500B might ruin the remainder of the chips

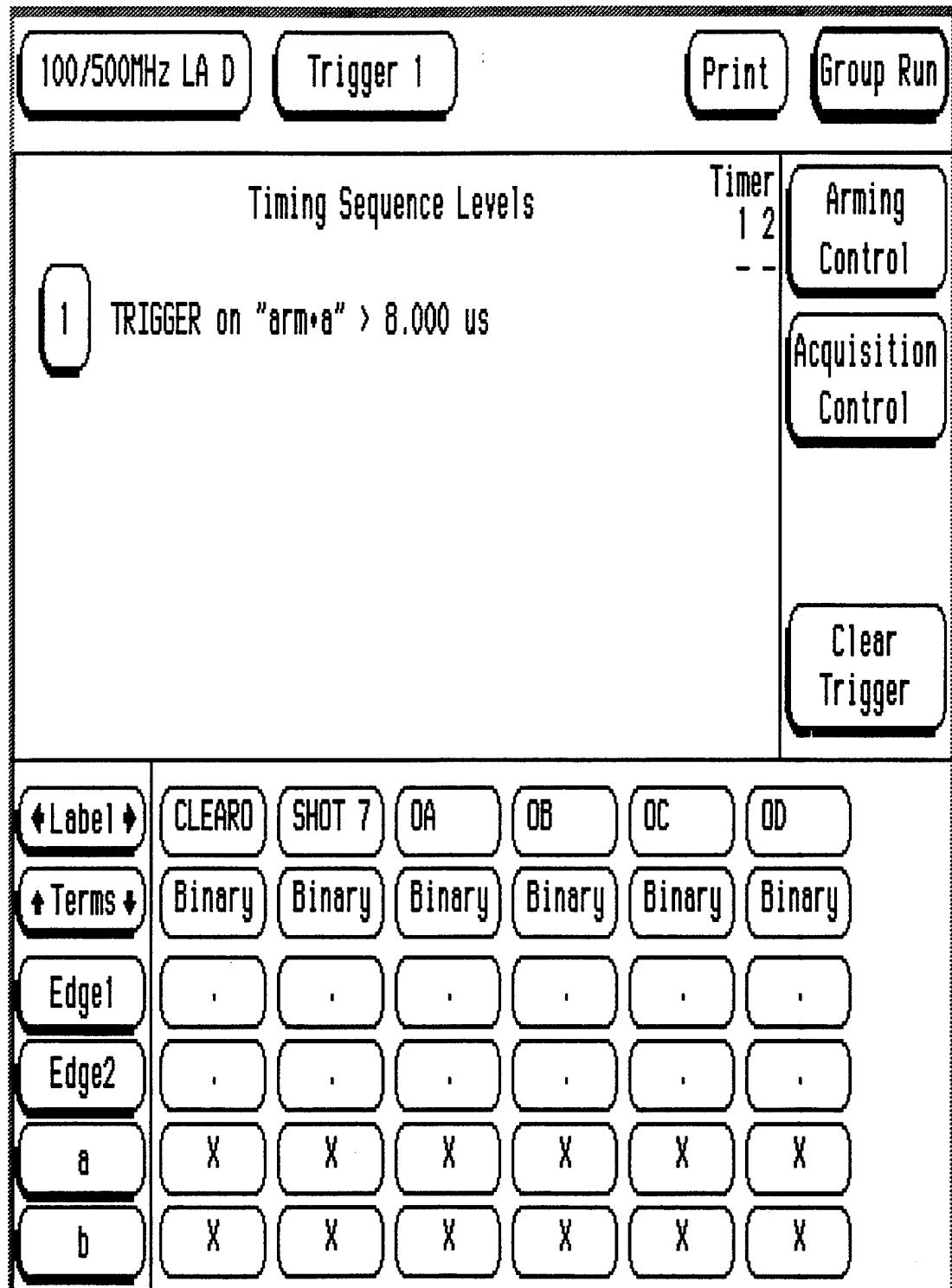


Figure 7. Trigger Settings on the Logic Analyzer

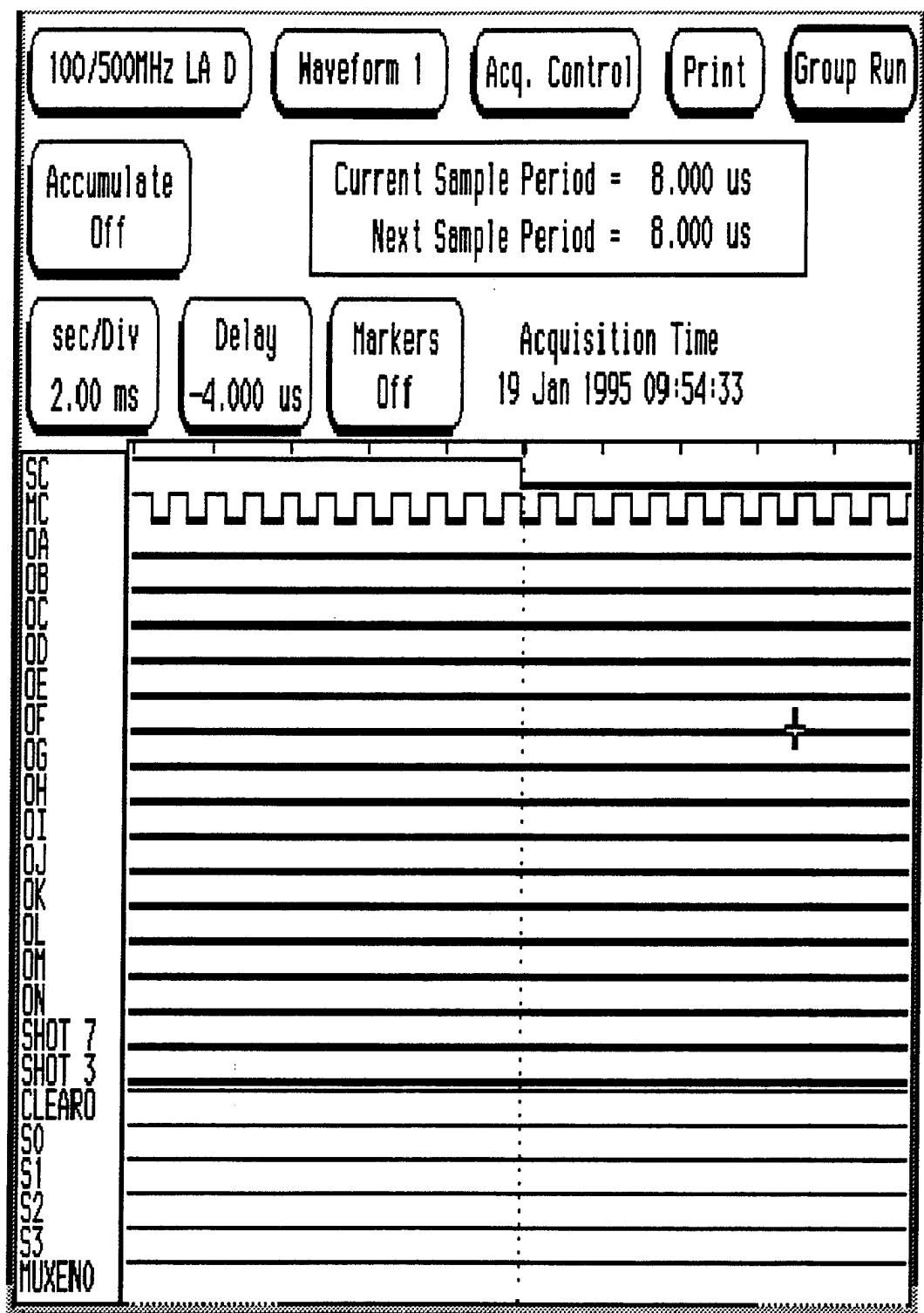


Figure 8. Chip 1 Waveforms

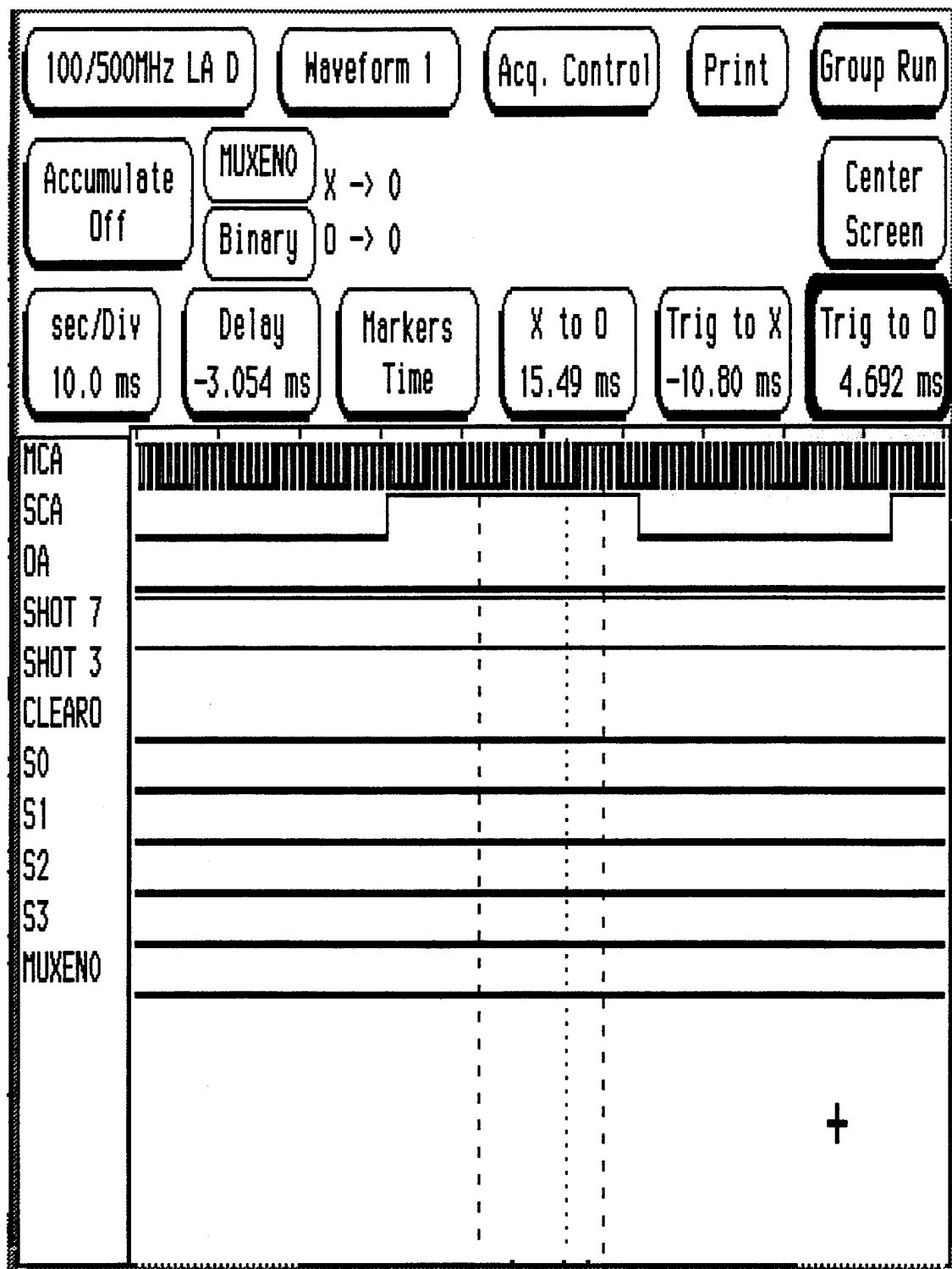


Figure 9. Chip 10 Waveforms

was considered. In hindsight, this proved to be a good decision because on the fifth chip tested we discovered many signal lines were generating outputs! This confirmed that the HP16500B was configured correctly. Figure 10 shows considerably more signal activity than do Figures 8 and 9. A careful analysis of Figure 10 will show that even this chip is not behaving as designed. Specifically, the data line, OA is a constant logic zero; the 3 and 7 stage one-shots never emit a pulse; S0, state zero from the FSM, has non-uniform pulses, and S2 is a constant logic one. Testing resumed in earnest with chips six through twelve. The cumulative results indicated that eight of the twelve chips had virtually no signal activity. Appendix C contains waveforms from tests of the remainder of the 2DHIST chips.

3. Event Simulation (ESIM) on the FSM

This test was done prior to fabrication but was repeated because the finite state machine is crucial to all operations in the histogram generation circuit. This logic is essentially the brains of the outfit. Without this logic working correctly, the chip is effectively dead. When so little was looking promising with test results, it was decided it would be prudent to rerun the ESIM test on the FSM.

ESIM is an event driven switch level simulator for CMOS transistor circuits. The ESIM user can issue a series of individual commands or direct ESIM to execute a batch file. There are commands to manipulate the network and others to control the simulation. [Ref. 10] See Figure 11 for the actual commands issued to ESIM and the data produced. The steps used to extract the FSM from the Magic layout and test it are as follows:

1. Box the cell to be extracted
2. Select the area
3. Select save <filename> {file will have .mag suffix}
4. Load <filename> {same as one generated in step 3 }
5. Extract {file will have .ext suffix}
6. Run ext2sim <filename> {file will have .sim suffix}
7. Run esim <filename> {same as one generated in step 6 }

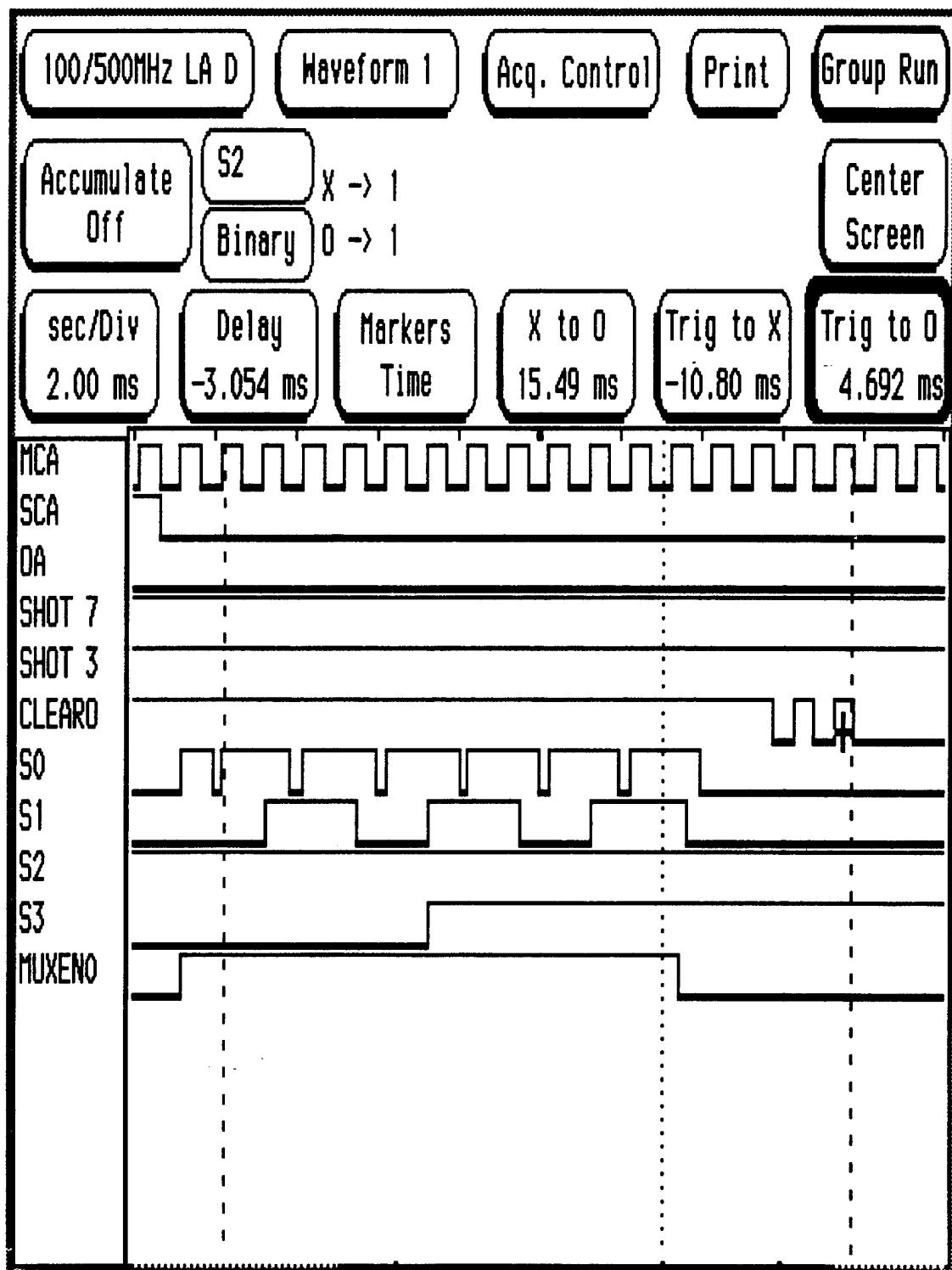


Figure 10. Chip 5 Waveforms

Figure 11. ESIM Test on the Finite State Machine

The value on each of the nodes of the input vectors are clocked through the FSM. Outputs are read in columns from left to right. The first run has several anomalies in the first two columns for the signals, S1, S3, muxen and clear. These are initialization errors. The commands used in ESIM are briefly explained. The command, "w" tells ESIM to watch the listed nodes. The "v" gives a view of the values on the watched nodes. Finally, "V" loads a vector and "G" is for go, which executes the simulation. What follows is [Ref. 11] and they are eliminated by rerunning ESIM. The number of initialization steps varied slightly (244 instead of 218) from Richstein's results [Ref. 12], but not appreciably. We offer no explanation as to why this occurred.

4. Latchup Test

Latchup is the destructive effect which can occur when a parasitic circuit exists in a CMOS process. Latchup is very detrimental because above a certain critical voltage, the circuit draws a large current while there is only a low voltage across the terminals. This condition is indicated on a plot when current goes up exponentially instead of staying approximately linear with voltage. The results of latchup are typically chip burnout, with the requirement to remove power to stop the current flow. Latchup can be prevented by adhering to proper layout techniques. [Ref. 13]

To determine if latchup was a problem, an ammeter was connected in series with the DC power supply to the 2DHIST IC chips. All equipment was connected to a common ground except the ammeter. The power supply output went to the current probe connection on the ammeter. The common connection of the ammeter was fed to all devices which required five volts. This setup kept the ammeter in series for an accurate set of current readings. Figure 12 shows the test bench configuration for this test. With 2DHIST chip number 1 in the ZIF socket, the power supply was energized. Voltage was stepped in one-tenth of a volt increments from zero to five volts. At each step the current was recorded and later plotted. The results of the latchup checks on three chips are shown in Figures 13 and 14. Refer to Appendix D to see the actual current data and the MATLAB program that was used to plot the results of the latchup tests. MATLAB is a

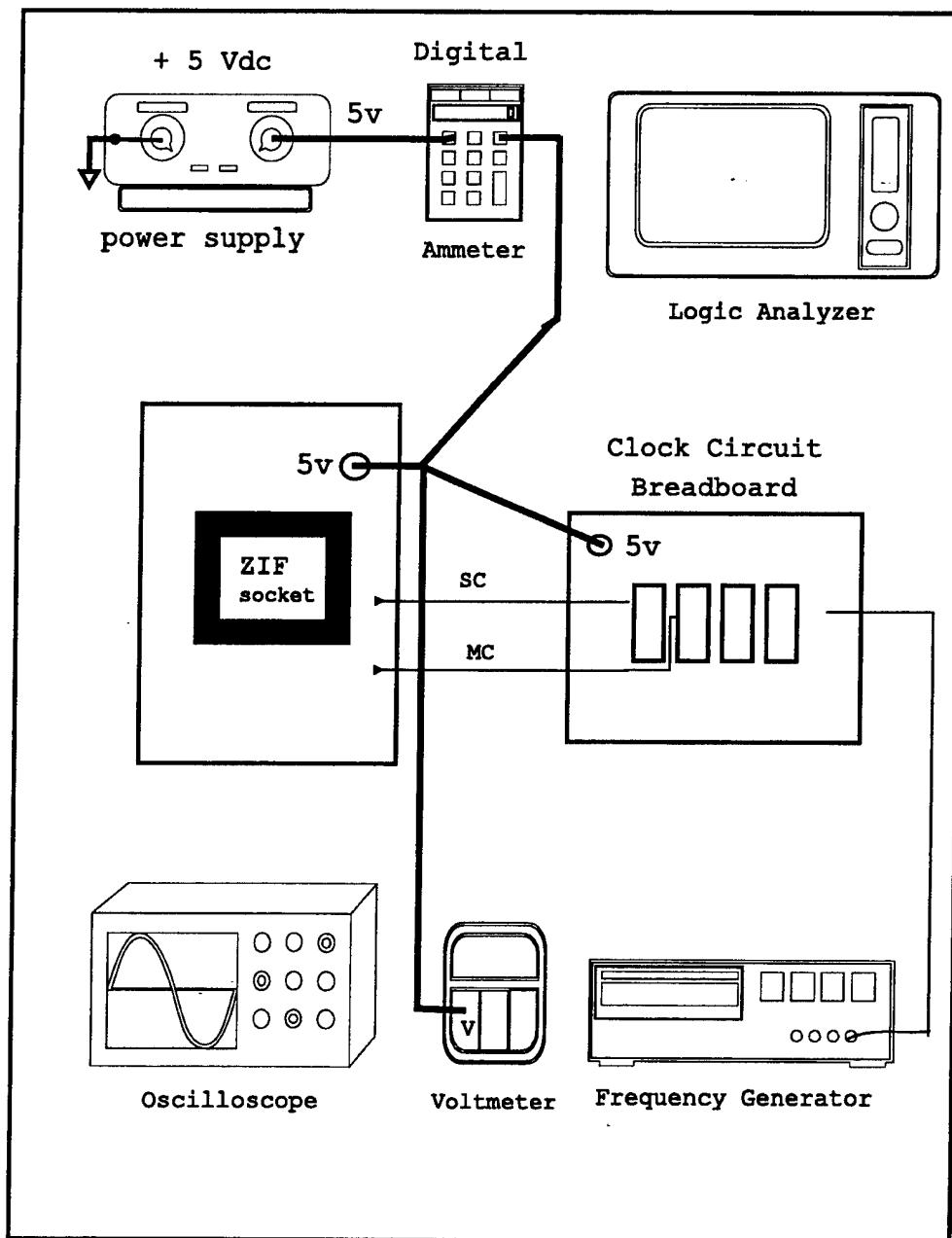


Figure 12. Latchup Test Setup

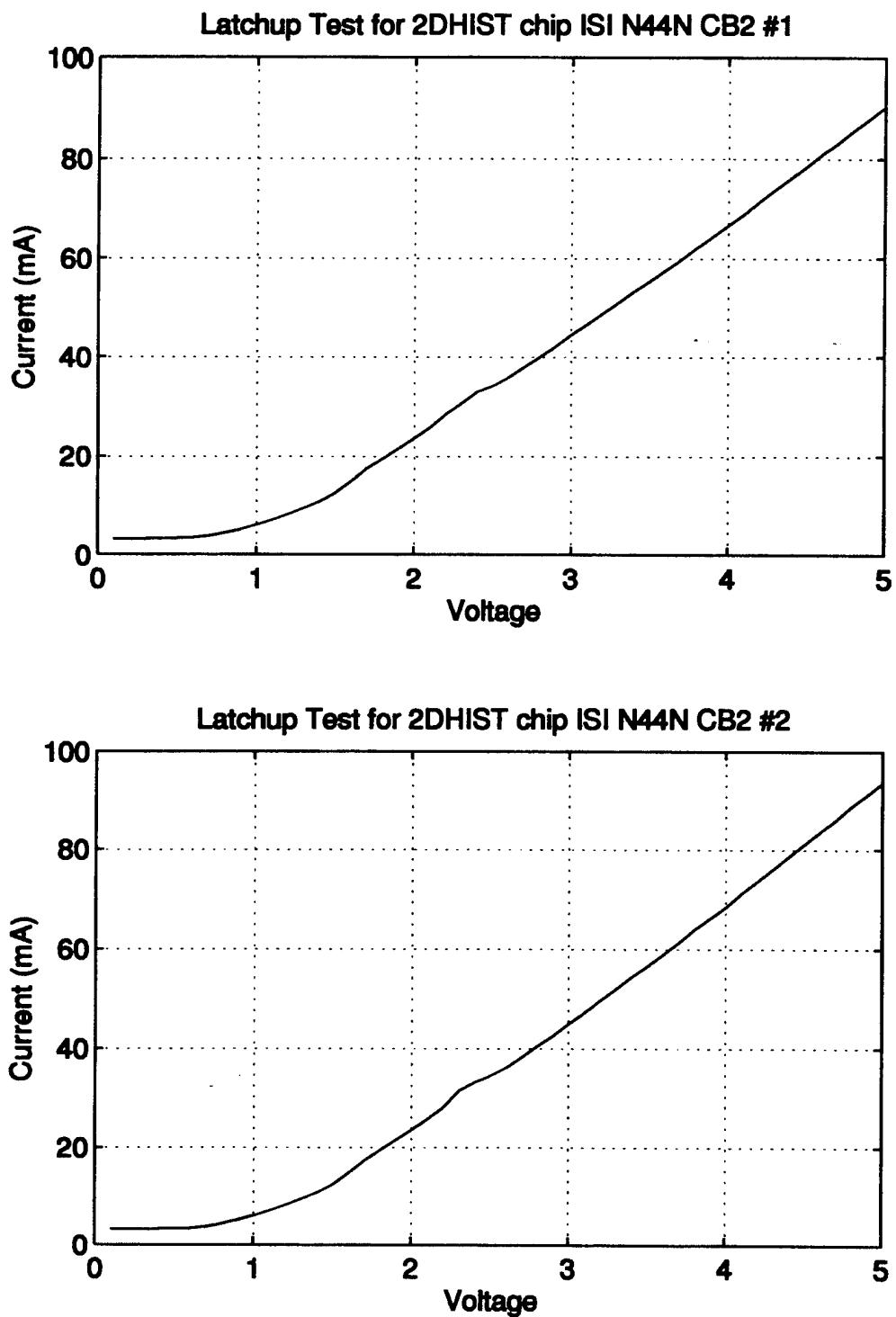


Figure 13. Latchup Results for Chips 1 and 2

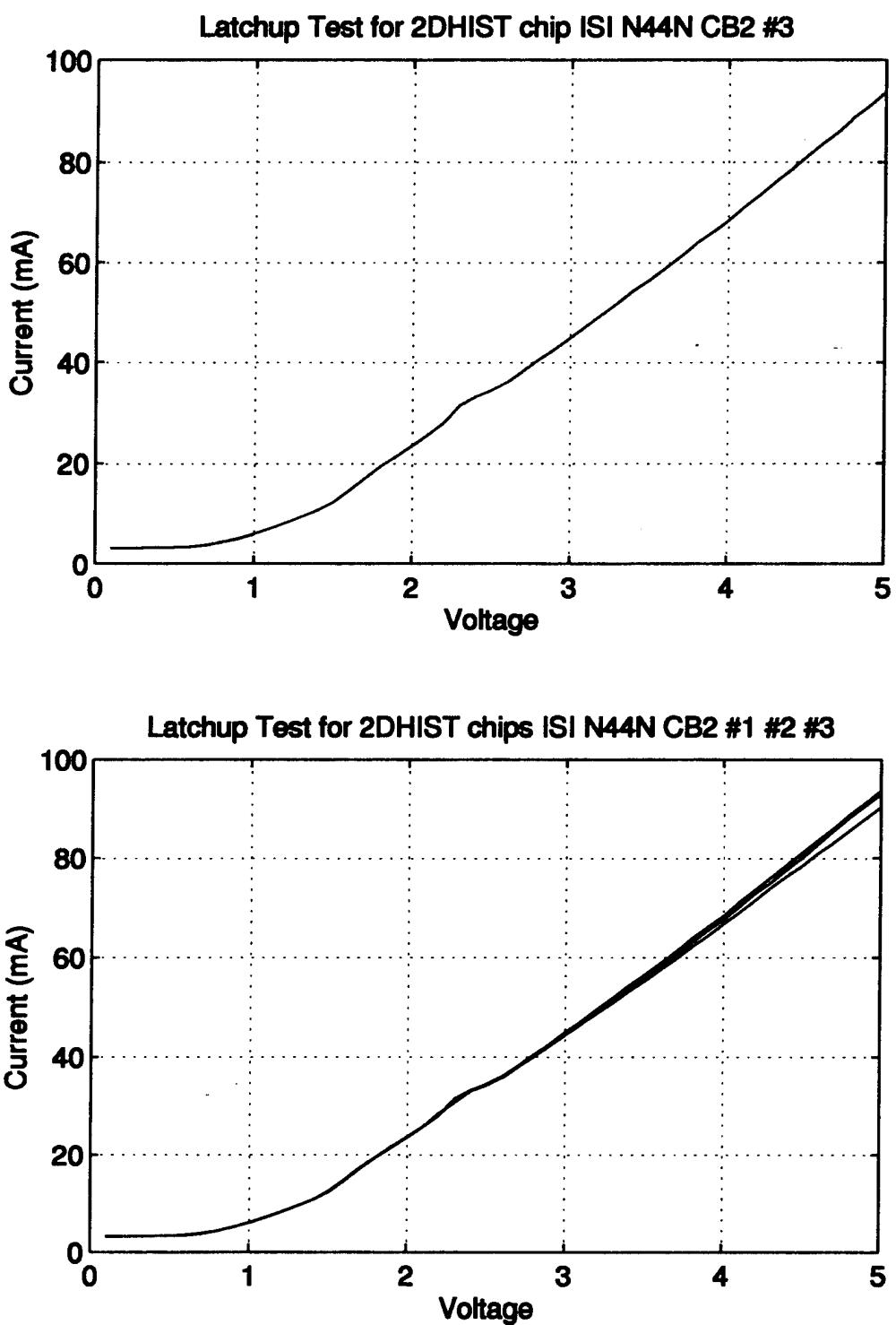


Figure 14. Latchup Results for Chip 3 and Chips 1, 2 & 3

technical computing software program for high-performance computation and visualization of matrix data [Ref. 14].

5. Verification of the Magic Layout

The 2DHIST designer used the software program Magic to layout the chip. Magic is an interactive system designed to simplify the creation and modification of VLSI circuits. At the Naval Postgraduate School, Magic runs on UNIX based SUN workstations. [Ref. 15]

In Magic, the layout was checked to ensure that all wells were connected to the substrate. These connections are referred to as substrate contacts, well plugs or well contacts [Ref. 16]. If there is not a contact in each well, then the probability of latchup increases. A methodical search of the entire 2DHIST layout was conducted to find any P-well that may not have been plugged. Similarly, this check was done for the N-wells. No omissions were found.

To accomplish this search many layers had to be turned off, leaving only the materials of interest visible. The steps followed to do this were:

1. :cif ostyle lambda = 1.0(pwell) {set the output style}
2. :see no {turn off all layers}
3. :see pwc {this is short for psubstratecontact}
4. :cif see cwp {show the pwell layer}
5. At this point a screen by screen check was made of the entire layout to ensure all p-wells were plugged.
6. :feedback clear {removes feedback information from the screen}
7. :cif ostyle lambda = 1.0(nwell) {set output style}
8. :see no {turn off all layers}
9. :see nwc {this is short for nsubstratecontact}
10. :cif see cwn {show the nwell layer}
11. At this point a screen by screen check was made of the entire layout to ensure all n-wells were plugged.

In Magic it is possible to shift the area of the layout being viewed by exactly one screenful. This is important to ensure that no area is skipped in a detailed visual search. Shifting by one screenful is done by clicking on the middle mouse button when the arrow is over the little squares at the ends of the scroll bars. [Ref. 17]

With all layers visible, another search was conducted to find any irregularities that may not have been detected by the electrical rule checker but still might have an adverse impact on the performance of the 2DHIST. The only thing askew was a small amount of polysilicon left dangling in the counters. This would have made a minor increase in the parasitic capacitance which would increase the delay in digital circuits [Ref. 18]. It would not explain the marginal performance of the 2DHIST chips though.

In Magic, labels are text strings attached to a cell's paint. Magic uses labels to provide information to other programs that process the circuit. Most labels are names of nodes. [Ref. 19] The search of the layout revealed that several labels were apparently misplaced. Specifically, there was no label on the pad in the upper left corner. "Vdd", the proper label for that pad, was placed there. Also, the label, "CLR" was on the buffer adjacent to the lowest 16-bit counter. This unnecessary label was removed. Given that this same layout file was extracted and successfully passed ESIM tests, we think these discrepancies are inconsequential.

6. Visual trace using the MicroManipulator

We conducted a visual trace of some key signal lines on the fabricated IC chip using the MicroManipulator Model 6100. This instrument is an analytical probe station and is used for scanning wafers and packaged devices. Manual controls allow precision movement in three dimensions. Submicron precision is possible when the device being tested is placed on the vacuum stage. The vacuum lines were not connected, nor were they necessary for our purposes. The MicroManipulator has the ability to magnify the image of an object up to 400 times. At high power magnification, only a small area can be viewed but with good resolution. The user can observe the object through the eyepiece or on a video monitor in real-time. [Ref. 20]

The MicroManipulator was used to perform a visual "continuity" check on several 2DHIST chips. Although expectations were not high, this instrument was readily available and afforded the opportunity to search for any obvious causes of failure. At approximately 400 times magnification, it is quite easy to visually trace circuit lines made of metal. We scanned several 2DHIST chips in this manner and found no broken metal paths or lines that did not match the Magic layout. Due to the relatively large surface area, only the signal lines and input/output pads for the FSM were examined.

C. TESTING SUMMARY

The 2DHIST was run through a battery of tests and failed to perform as designed. The continuity test passed but the HP Pattern Generator Tests revealed serious problems with all chips. When ESIM was rerun for verification, the results matched the designers' results. The latchup test data indicated the 2DHIST ICs did not have a latchup condition. Similarly, the Magic design layout was checked and no defects were noted. Finally, a visual trace of a key part of the IC failed to reveal any obvious fabrication errors.

IV. PSPICE SIMULATION OF THE 1DHIST CIRCUIT

A. CONCEPT VALIDATION FOR 2DHIST

The intent of running a Pspice simulation of the 1DHIST circuit was to show that the histogram generation concept is valid. This was deemed to be relevant when the testing results were dismal. By demonstrating via breadboard and simulation that the 1DHIST gives meaningful data in real-time, the concept merited extending to a two directional scan.

Pspice is a CAD program that allows circuit design and simulation for both analog and digital circuits. It consists of several programs that aid the engineer. The program Schematics is for laying out the components in a design. The Parts program was used to model a diode not found in the Pspice library. The FJT1100 is a low leakage type diode and parameters from Fairchild data sheets were used to create this model. Pspice itself is the simulation program which was used here because it can simulate a circuit with both analog and digital components. The Probe program was for observing the waveforms produced by the simulation. The Pspice 5.0a package was run on a SUN workstation. [Ref. 21]

The 2DHIST is a more accurate 12-bit version of the 1DHIST. In the original design, the best resolution was 256 samples. With more counters, 12 versus 8, and larger counters, 16 bits versus 8 bits, the resolution is significantly enhanced. The 2D is capable of a maximum sample size of $2^{16} = 65,536$ samples, or 2^8 samples in the X direction and 2^8 samples in the Y direction. This translates to a resolution of 256 x 256 samples for the object being scanned. [Ref. 5] Since each counter generates a 16-bit word, 16 multiplexers (MUX) are required. For example, bit 0 of counter 0 would be gated to MUX 0, bit 1 of counter 0 would be sent to MUX 1, and so on for the remaining 14 bits of each counter.

B. COMPONENTS

The components used in the Pspice simulation of the 1DHIST nearly matched those used to build the prototype. This close correspondence allows a meaningful

comparison between results from the simulation and the data gathered earlier on the breadboard version of the 1DHIST circuit. The primary difference is that in the Pspice model, all resistors, capacitors and power supplies are ideal. Table 2 identifies the components used on the breadboard and for the Pspice simulation.

Device	Breadboard part number	Pspice part number	Notes
counter	74LS193	74LS193	sync 4-bit binary up/down counter
counter	74LS393	74LS393	sync 4-bit binary counter
diode	FJT1100	FJT1100	user defined in PARTS program for Pspice
diode	FSA2510P	MR25110M	
D flip flop	74LS74A	74LS74A	
inverter gate	74LS04	74LS04	needed to implement '393 as an 8-bit counter
one-shot	74LS123	74LS123	R=10KΩ , C=5nF. No external RC for Pspice but set attribute, TC = 50 μs.
op-amp	LM 324	LM 324	
op-amp	LM 347	LM 347/TI	
op-amp	LM 356	LM 356/LT	
AND gate	74LS08	74LS08	2-inputs
AND gate	74LS21	74LS21	4-inputs
OR gate	74LS02	74LS02	2-inputs
XOR gate	74LS86	74LS86A	
MUX	74LS151	74LS251	8 to 1 multiplexer

Table 2. Circuit Components

C. SIMULATION RESULTS

The 1DHIST schematics that were drawn using the schematic capture ability of the program Schematics are shown in Appendix E. The components are those discussed in Chapter II. Differences between the simulation parts and those used in laboratory are minor. The primary test run on this circuit was a transient analysis. This is a very computationally intensive test, even for this modest circuit of less than 900 nodes. Several iterations were run of varying execution times. The Pspice program files are included in Appendix E.

The stimulus used in lieu of actual photodetector output was a time varying, 0 volts to 5 volts square wave. In fact, it is identical to the PC waveform. This is similar to the stimulus used previously on a physical model of the 1DHIST circuit.

Many difficulties were encountered with the simulation of the 1DHIST. These are primarily due to the simulation tool, Pspice and to a lesser extent because of Schematics. Circuit layout type problems encountered were, undefined subcircuits for parts in the device model libraries and devices from the library not matching manufacturer's data sheets. The reason these undefined parts are included by MicroSim is only to facilitate drawing of schematics [Ref. 21]. One case where an IC does not match the data sheets is the 74LS393. IEEE standards indicate this should be drawn as a dual 4-bit binary counter; it is drawn as a single 4-bit counter.

The effects of these shortcomings are two-fold. First, the parts library was checked for availability of the components in Table 2 before Pspice 5.0a was selected as the simulation tool. This was done to ensure it could model all the parts used with the 1DHIST laboratory experiment. The result was that substitutions had to be made when undefined parts were discovered. Second, the schematics in Figures 22 and 23 differ because of Pspice's model variations (i.e., the 74LS393). This forced an altered design to accommodate these variances.

Pspice is the program that stimulates a schematic design and records values over time at the nodes. The difficulties it posed were due to extremely sensitive edge triggering

requirements, its occasional erratic behavior, and its disposition to crash without explanation. The digital devices, specifically, the 74LS193 counter as modeled required extremely sharp edges to function. Rise times had to be approximately 5 ns or the device outputs would remain indeterminate. The most frequent erratic behavior noted was when a digital device, from the parts library, would appear with distorted graphics in the schematic. The box that normally outlines the device would be literally all over the screen. Needless to say, this greatly impeded circuit layout changes although the schematic would still pass the electrical rule check. Another malfunction that remains unexplainable is that during many instances, Pspice would run however, it would record no data. The data results file labeled as *schematic_filename.DAT*, would be of size zero after running for over 100 microseconds. Occasionally, these simulation errors would go away by closing and reopening the file, other times by exiting the program or logging off the workstation.

MicroSim's technical support department initially provided quick and helpful replies to short, concise problems. Often though, we needed to go back and tell MicroSim that the proposed solution was not applicable to version 5.0. The fix was based on the newer release, version 6.1.

In summary, due to time constraints and the problems posed by the simulation software meaningful simulation data was not gathered. The Pspice files, including the netlist, alias, circuit, and output are included in Appendix E because they represent the traditional SPICE deck. The intention here is that the research may continue using another simulation program but continuing from this point instead of starting all over.

V. RESULTS

A. CONCLUSIONS

The testing results are admittedly disappointing since none of the 2DHIST chips functioned as they were designed. Of the four chips that had significant activity, none behaved quite like any of the other chips. Furthermore, not one of the twelve 2DHIST chips functioned as it was designed!

After checking continuity, testing for latchup, verifying the Magic layout, running tests with a logic analyzer system, and conducting several simulations and finding no consequential errors, we conclude that the 2DHIST IC chips were designed correctly. Our conclusion is that this batch of IC chips are most likely defective due to faulty fabrication.

B. LESSONS LEARNED

After conducting this battery of tests, there are some lessons learned that may be of interest to others embarking on a test related project. These are offered in no particular order.

- ◆ Recheck all connections. Whether electrical lines are joined by wire wrap, alligator clips, solder or other connectors, close physical proximity does not guarantee a good electrical connection. Continuity checks with an ohm meter can determine if lines are properly mated. When a connection is suspect, rewrap, resolder or disconnect and reconnect the lines. There may have been oxidation on the surfaces.

- ◆ Seek technical support early and often. Do not let pride be the enemy of progress. When a software program is not behaving the way the documentation indicates, contact an expert user or the company's product support department. There may be undocumented bugs which they know how to correct or work around. Find the most expedient method to initiate the request for help; just because it is a personal crisis does not necessarily make it a priority for others.

- ◆ Use only software that has stood the test of time for any project of considerable magnitude.

- ◆ Question the paradigms. When something seems right but just will not work and everything has been checked, step back and try to find a radically different method to solve the problem.
- ◆ Write down all assumptions made and verify these with an expert. A wrong assumption made at an early stage could cause a lot of wasted time and effort.
- ◆ Redo key simulations. When test results do not match the expected results, it may be instructive to repeat the simulations.
- ◆ Question inconsistencies. This may unravel the problem. Some things truly are among the mysteries of life but most problems have answers if enough time is spent seeking them. Wisdom lies in knowing which to pursue and which to accept.

C. FURTHER RESEARCH

Porting the Pspice version of SPICE code to another simulation program may achieve the concept validation for the 2DHIST that was attempted here. Other than that though, no more testing needs to be done on the 2DHIST chips. When funds become available, the 2DHIST layout should be resubmitted for fabrication. It may be instructive to redesign the one-shot before this. Since the one-shot was only tested in Spice, it may not function as designed. Another item to pursue is converting more of the analog to digital conversion circuit shown in Chapter II to VLSI. This would make the overall system smaller and more modular. Weste [Ref. 22] discusses this process for a six-bit example which could easily be extended.

APPENDIX A. MOSIS TECHNICAL REPORT

A. MOSIS PARAMETRIC TEST RESULTS

RUN: N44N

VENDOR: ORBIT

TECHNOLOGY: SCPE20

FEATURE SIZE: 2.0 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of the MOSIS test structures on each wafer of this fabrication lot. The SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: This looks like a typical Orbit Semiconductor 2.0um p-well run.

TRANSISTOR PARAMETERS		W/L	N-CHANNEL P-CHANNEL UNITS	
MINIMUM		3/2		
Vth			1.03	-0.78 Volts
SHORT		18/2		
Vth			0.93	-0.75 Volts
Vpt			16.2	-11.0 Volts
Vbkd			16.1	-15.3 Volts
Idss			2610	-1359 uA
LARGE		50/50		
Vth			0.92	-0.78 Volts
Vbjkd			16.0	-18.1 Volts
Ijlk			-17.2	-5.2 pA
Gamma			1.09	0.44 V ^{1/2}
Delta length (L_eff = L_drawn-DL)			0.64	0.44 microns
Delta width (W_eff = W_drawn-DW)			-0.42	-0.06 microns
K' (Uo*Cox/2)			25.8	-10.2 uA/V ²
POLY2 TRANSISTORS		W/L	N-CHANNEL P-CHANNEL UNITS	
MINIMUM		6/4		
Vth			1.05	-0.99 Volts
SHORT		36/4		
Vth			0.98	-0.95 Volts
LARGE		36/36		
Vth			0.96	-0.97 Volts

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	20.7	-12.3	Volts
PROCESS PARAMETERS N+DIFF P+DIFF N+POLY P+POLY POLY2 M1 M2 UNITS				
Sheet Resistance	28.2	74.8	20.5	23.0 21.4 0.05 0.03 Ohms/sq
Width Variation (measured - drawn)	0.00	-0.17	-0.25	-0.19 -0.21 -0.01 0.52 microns
Contact Resistance	42.8	38.8	10.2	13.1 13.1 0.04 Ohms
Gate Oxide Thickness	383			Angstroms
CAPACITANCE PARAMETERS N+DIFF P+DIFF POLY POLY2 M1 M2 UNITS				
Area (substrate)	428	211	60	44 27 aF/um ²
Area (poly)				483 45 26 aF/um ²
Area (poly2)				46 aF/um ²
Area (metall1)				35 aF/um ²
Area (N+active)			871	48 27 aF/um ²
Area (P+active)			862	aF/um ²
Fringe (substrate)	600	86		aF/um
Fringe (N+active)			47	aF/um
Fringe (P+active)			77	aF/um
CIRCUIT PARAMETERS UNITS				
Inverters	K			
Vinv	1.0	2.22	Volts	
Vinv	1.5	2.43	Volts	
Vlow	2.0	0.00	Volts	
Vhigh	2.0	4.99	Volts	
Vinv	2.0	2.58	Volts	
Gain	2.0	-10.95		
Ring Oscillator				
MOSIS (31 stages)		35.97	MHz	

N44N SPICE LEVEL 2 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.0000E-08 XJ=0.200000U
+ TPG=1VTO=0.9260 DELTA=9.0900E+00 LD=3.2080E-07 KP=4.9587E-05
+ UO=574.4 UEXP=1.8260E-01 UCRIT=7.1070E+04 RSH=1.8190E+01
+ GAMMA=1.0015 NSUB=2.2520E+16 NFS=7.6500E+12 VMAX=6.6450E+04
+ LAMBDA=2.7590E-02 CGDO=4.1541E-10 CGSO=4.1541E-10
+ CGBO=4.1409E-10 CJ=4.3565E-04 MJ=0.4572 CJSW=5.1849E-10
+ MJSW=0.310317 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1900E-07
```

```

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.0000E-08 XJ=0.200000U
+ TPG=-1 VTO=-0.7378 DELTA=2.0960E+00 LD=2.1830E-07 KP=2.0563E-05
+ UO=238.2 UEXP=3.2750E-01 UCRIT=8.2670E+04 RSH=2.2000E+01
+ GAMMA=0.5338 NSUB=6.3960E+15 NFS=4.5480E+10 VMAX=9.9990E+05
+ LAMBDA=5.0840E-02 CGDO=2.8268E-10 CGSO=2.8268E-10
+ CGBO=3.5474E-10 CJ=2.0844E-04 MJ=0.4462 CJSW=1.1163E-10
+ MJSW=0.07452 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.7400E-08

```

```

N44N SPICE BSIM PARAMETERS NM1 PM1 DU1 DU2 ML1 ML2
*
*PROCESS=ORBIT
*RUN=n44n
*WAFER=44
*Gate-oxide thickness= 400 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 3.0/2.0, 6.0/2.0, 18.0/2.0, 18.0/5.0, 18.0/25.0
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=8-Jun-1994
*
*NMOS PARAMETERS
*
-8.71358E-01,-7.92999E-03,-1.14389E-02
7.71652E-01, 0.00000E+00, 4.26619E-24
1.14314E+00, 1.00532E-01, 5.26987E-01
6.78840E-04, 1.11142E-01, 4.23092E-03
-3.50453E-03, 1.82001E-02,-5.87070E-04
5.69841E+02,8.51957E-001,1.30479E-002
5.38565E-02, 7.43907E-02,-5.21613E-02
2.70936E-02, 4.66513E-01,-2.84730E-01
1.46270E+01,-2.86586E+01, 5.42396E+01
-1.40892E-04,-7.93754E-03,-3.32880E-03
2.61093E-04,-2.46823E-03,-4.43706E-03
2.60418E-03,-1.37314E-02, 3.33310E-02
-1.79145E-03, 8.57289E-03, 3.79473E-03
5.41689E+02, 3.54971E+02,-7.48009E+01
5.73278E+00,-1.73387E+01, 8.98372E+01
-3.11103E+00, 5.89586E+01,-2.43118E+01
-2.89238E-03, 5.14917E-02,-8.96860E-03

```

```

4.00000E-002, 2.70000E+01, 5.00000E+00
5.51612E-010, 5.51612E-010, 3.48583E-010
1.00000E+000, 0.00000E+000, 0.00000E+000
1.00000E+000, 0.00000E+000, 0.00000E+000
0.00000E+000, 0.00000E+000, 0.00000E+000
0.00000E+000, 0.00000E+000, 0.00000E+000
*
* Gate Oxide Thickness is 400 Angstroms
*
*
*PMOS PARAMETERS
*
-3.39633E-01, -6.23482E-03, 2.07480E-01
6.59116E-01, -9.60429E-25, 0.00000E+000
5.21747E-01, -3.40905E-02, -1.43993E-01
2.04072E-02, 4.31714E-02, -1.06851E-01
-1.00978E-02, 7.59870E-02, -1.74019E-02
2.23249E+02, 6.39871E-001, -4.62627E-002
1.24519E-01, 4.55750E-02, -9.03951E-02
3.97257E-02, 2.36316E-01, -9.97538E-02
8.56606E+000, -2.57316E+000, 6.79918E+000
-2.35051E-004, -1.65815E-03, -5.89308E-03
4.43259E-04, -3.99724E-03, 2.81393E-03
4.74412E-03, 5.99036E-04, 4.21784E-03
2.36240E-03, -4.57513E-03, 1.52887E-02
2.44413E+02, 1.14819E+02, -3.16686E+01
8.35928E+000, -5.87882E-01, 1.58473E+01
3.62403E-01, 1.46103E+01, -1.15146E+01
-1.50656E-02, 2.90576E-03, 4.21141E-03
4.00000E-002, 2.70000E+01, 5.00000E+000
4.14294E-010, 4.14294E-010, 3.52909E-010
1.00000E+000, 0.00000E+000, 0.00000E+000
1.00000E+000, 0.00000E+000, 0.00000E+000
0.00000E+000, 0.00000E+000, 0.00000E+000
0.00000E+000, 0.00000E+000, 0.00000E+000
*
*N+ diffusion::
*
28.2, 4.356500e-04, 5.184900e-10, 1.000000e-08, 0.8
0.8, 0.457249, 0.310317, 0, 0
*
```

```

*P+ diffusion::
*
74.8, 2.084400e-04, 1.116300e-10, 1.000000e-08, 0.7
0.7, 0.446161, 0.07452, 0, 0
*
*METAL LAYER -- 1
*
5.000000e-02, 2.600000e-05, 0, 0, 0
0, 0, 0, 0, 0
*
*METAL LAYER -- 2
*
3.000000e-02, 1.300000e-05, 0, 0, 0
0, 0, 0, 0, 0

```

B. ORBIT ELECTRICAL PARAMETERS

*** this file was downloaded from the MOSIS World Wide Web (WWW)

*** homepage at <http://info.broker.isi.edu:80/mosis/vendors/orbit-scpe20>

*** as of 8 March 95 under the link to scpe20-orbit-specs.inf

(2UM, 2 METAL, 2 POLY, P-WELL CMOS WITH 2ND POLY MAKING XTORS)

A.1 Oxide Thicknesses (Angstroms)

		MIN	TYP	MAX
		---	---	---
A.1.1	Poly 1 gate oxide	370	400	430
A.1.2	Poly 2 gate oxide	470	500	530
A.1.3	Field oxide (Poly 1 & 2 to Sub)	5500	6000	6500
A.1.4	Metal 1 to Poly 1 & 2	8000	8500	9000
A.1.5	Metal 1 to Sub	13500	14500	15500
A.1.6	Metal 1 to N+/P+ Diff	8500	9000	9500
A.1.7	Metal 2 to Metal 1	6000	6500	7000
A.1.8	Poly 1 to Poly 2	650	750	850

A.2 Conductors

A.2.1	Poly 1	3700	4000	4300
A.2.2	Poly 2	3700	4000	4300
A.2.3	Metal 1	5500	6000	6500
A.2.4	Metal 1	10500	11500	12500

B. TRANSISTOR SPECIFICATIONS

B.1 P Channel Poly 1

B.1.1	Threshold (volts)	-1.0	-0.75	-0.5
B.1.2	Gamma (volts $^{1/2}$)	0.2	0.4	0.6
B.1.3	$K' = uCox/2 \text{ (uA/v}^2\text{)}$	6.0	7.5	8.5
B.1.4	Punchthrough for min. length channel (volts)	-16	-14	-10
B.1.5	Subthreshold slope (millivolts/decade)	90	100	110
B.1.6	Delta width = effective-mask (microns)	-0.8	-0.9	-1.2
B.1.7	Delta length = effective-mask (microns)	-0.8	-0.3	0

B.2 P Channel Poly 2

B.2.1	Threshold (volts)	-1.6	-1.25	-1.0
B.2.2	Gamma (volts $^{1/2}$)	0.3	0.45	0.6
B.2.3	$K' = uCox/2 \text{ (uA/v}^2\text{)}$	5.0	6.0	7.0
B.2.4	Punchthrough for min. length channel (volts)	-16	-14	-10
B.2.5	Subthreshold slope (millivolts/decade)			
B.2.6	Delta width = effective-mask (microns)	-0.6	-0.9	-1.2
B.2.7	Delta length = effective-mask (microns)	-0.8	-0.5	-0.2

B.3 N Channel Poly 1

B.3.1	Threshold (volts)	0.5	0.75	1.0
B.3.2	Gamma (volts $^{.5}$)	0.5	0.7	1.2
B.3.3	$K' = ucox/2 \text{ (uA/v}^2\text{)}$	20	23	26
B.3.4	Subthreshold slope (millivolts/decade)	90	100	110

B.3.5	Punchthrough for min. length channel (volts)	10	14	16
B.3.6	Delta width = effective-mask (microns)	-0.8	-0.9	-1.2
B.3.7	Delta length = effective-mask (microns)	-0.7	-0.4	-0.1
B.4 N Channel Poly 2				
B.4.1	Threshold (volts)	0.75	0.95	1.25
B.4.2	Gamma (volts^.5)	0.7	0.9	1.1
B.4.3	K'=uCox/2 (uA/v^2)	18	20	22
B.4.4	Subthreshold slope (millivolts/decade)	90	100	110
B.4.5	Punchthrough for min. length channel (volts)	10	14	16
B.4.6	Delta width = effective-drawn (microns)	-0.6	-0.9	-1.2
B.4.7	Delta length = effective-drawn (microns)	-0.9	-0.6	-0.3

C. SHEET RESISTANCES (OHMS PER SQUARE)

		MIN	TYP	MAX
		---	---	---
C.1	P+ Active	50	70	100
C.2	N+ Active	15	22	30
C.3	P Well (with field implant)	1800	2200	3000
C.4.1	Poly1	15	21	30
C.4.2	Poly2	20	28	35
C.5	Metal1	.050	.070	.090
C.6	Metal2	.030	.040	.050

D. CONTACT RESISTANCE (OHMS)

D.1	Metal1 to P+ Active	35	75
D.2	Metal1 to N+ Active	20	50
D.3.1	Metal1 to Poly1	20	50
D.3.2	Metal1 to Poly2	20	50

D.4 Metall1 to Metal2 0.4 0.7
(single contact 2 by 2um)

E. FIELD INVERSION AND BREAKDOWN VOLTAGES (VOLTS)

E.1.1	N Channel Poly1 field inversion	10	14
E.1.2	N Channel Poly2 field inversion	10	14
E.2	N Channel Metal1 field inversion	10	15
E.3	N Channel Metal2 field inversion	-	-
E.4.1	P Channel Poly1 field inversion	-12	-10
E.4.2	P Channel Poly2 field inversion	-12	-10
E.5	P Channel Metal1 field inversion	-12	-10
E.6	P Channel Metal2 field inversion	-	-
E.7	N diffusion to substrate junction breakdown	14	16
E.8	P diffusion to substrate junction breakdown	15	18
E.9	N-well to P-substrate junction breakdown	50	90

INTERLAYER CAPACITANCES

(PLATE: 10 ** -5 PF / MICRON ** 2 FRINGE: 10 ** -5 PF / MICRON)

	Capacitance		Equiv. Thickness	
	MIN	MAX	MIN	MAX
GATE OXIDE PLATE POLY1	75	90	370 Ang	430 Ang
GATE OXIDE PLATE POLY2	64	70	470 Ang	530 Ang
FIELD POLY1 TO SUBS FRINGE				
FIELD POLY2 TO SUBS FRINGE				
POLY1 TO POLY2 OVER ACTIVE	43	55	650 Ang	850 Ang
POLY1 TO POLY2 OVER FIELD	43	55	650 Ang	850 Ang
METAL1 TO ACTIVE PLATE	3.6	4.0	8500 Ang	9000 Ang

METAL1 TO ACTIVE FRINGE

METAL1 TO SUBS PLATE 2.2 2.5 13500 Ang 15500 Ang

METAL1 TO POLY PLATE 3.7 4.4 8000 Ang 9000 Ang

METAL1 TO POLY FRINGE

METAL2 TO ACTIVE PLATE 1.9 2.4 14500 Ang 17500 Ang

METAL2 TO ACTIVE FRINGE

METAL2 TO SUBS PLATE 1.5 1.65 19500 Ang 22000 Ang

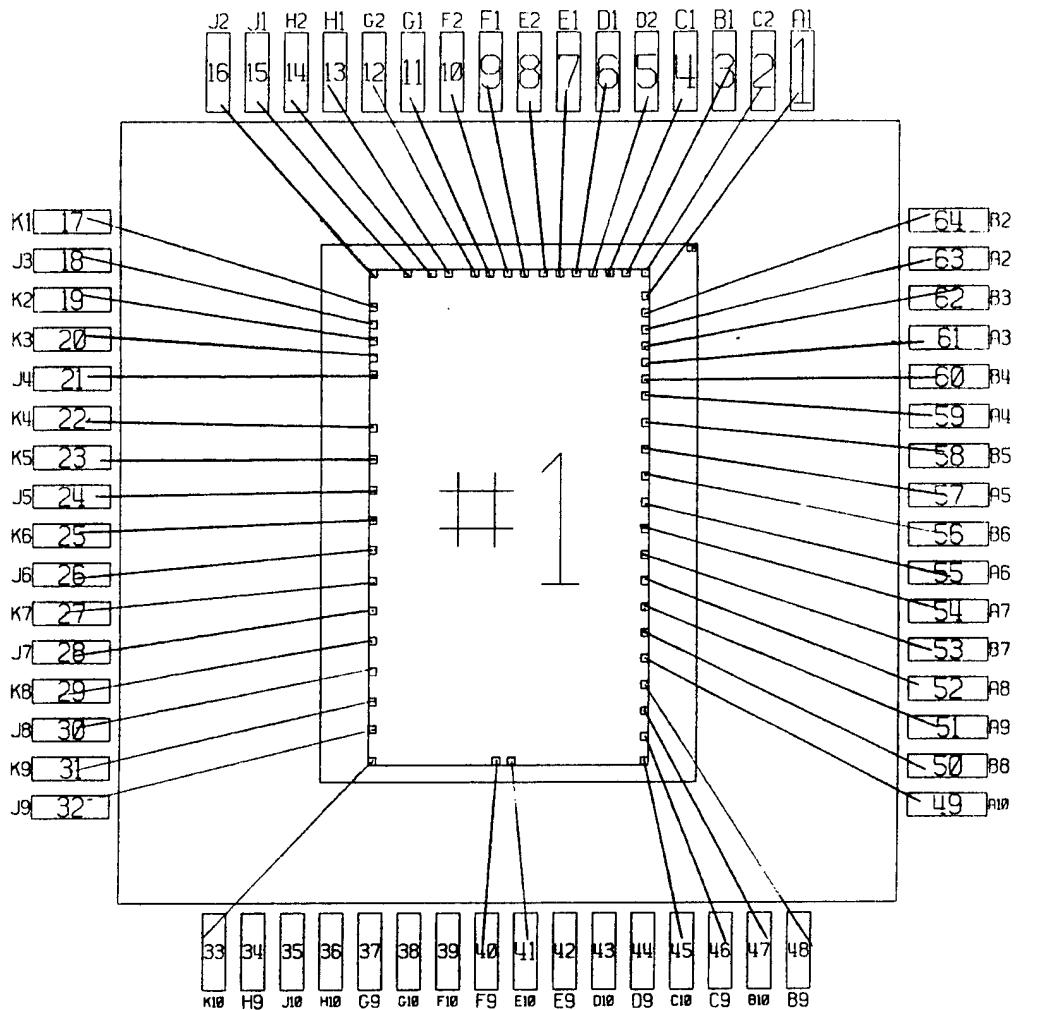
METAL2 TO SUBS FRINGE

METAL2 TO POLY PLATE 1.9 2.4 14500 Ang 17500 Ang

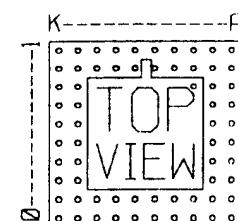
METAL2 TO POLY FRINGE

METAL2 TO METAL1 PLATE 4.6 5.6 6000 Ang 7500 Ang

METAL2 TO METAL1 FRINGE



N44NCB 2
920-NSF-ACLAS/NPS
#1: 42566/Fouts/STATARITH



PGA65: 12 PARTS
14-APR-1994

Figure 15. Bond Pad Layout

APPENDIX B. PINOUT FOR 2DHIST IC CHIP

A. PINOUT AND ASSOCIATED FUNCTIONS

The following table gives the correspondence between the pin numbers on the 65 lead PGA and the signal labels assigned by the designer in MAGIC, the CAD layout program.

The layout package submitted by Richstein [Ref. 5] has only 64 usable leads. Pin C3 was not assigned in the layout sent to MOSIS, however, the fabricator opted to connect pins C2 and C3. Wes Hansford at MOSIS explained this was done because they offer as a standard part a 65 lead PGA. The 65th lead is an index pin which is connected to pin 2. We believe the effect of this was not detrimental. It merely put 5 volts on pin C3 and that was expected since pin C2 is connected to Vdd. We put no jumpers or leads on pin C3 for the tests.

To eliminate any confusion the pins named, MC and MCA, require the same clock input. The designer put separate input pins for the same signal to avoid adding considerable wiring interconnect which would have been required to internally pass the clock signal in the 2DHIST layout. For similar reasons, the same is true for the SC and SCA signals.

Pin number	Name	Function
A1	MUXENOUT	MUX enable output, from finite state machine (FSM)
A2	S3OUT	state S3 output, from FSM
A3	OA	least significant bit of output
A4	OC	output bit
A5	OE	output bit
A6	OG	output bit
A7	OH	output bit

Pin number	Name	Function
A8	OJ	output bit
A9	OK	output bit
A10	OM	output bit
B1	S2in	state S2, input to MUX
B2	MUXENIN	input for MUX enable
B3	S3in	state S3, input to MUX
B4	OB	output bit
B5	OD	output bit
B6	OF	output bit
B7	OI	output bit
B8	OL	output bit
B9	ON	output bit
B10	OO	output bit
C1	S2OUT	state S2 output, from FSM
C2	Vdd	pad ring power
C3		none
C9	OP	most significant bit of output
C10	GND	pad ring ground
D1	S1OUT	state S1 output, from FSM
D2	S1in	state S1, input to MUX
D9		none
D10		none

Pin number	Name	Function
E1	S0in	state S0, input to MUX
E2	S0OUT	state S0 output, from FSM
E9		none
E10	GND	chip ground
F1	MC	master clock
F2	SC	scan clock
F9	Vdd	chip power
F10		none
G1	Vdd	chip power
G2	GND	chip ground
G9		none
G10		none
H1	CLEAROUT	clear signal, output from FSM
H2	CLEARIN	clear signal, input to chip
H9		none
H10		none
J1	BGOUT	seven delay one-shot output
J2	Vdd	pad ring
J3	SCA	scan clock
J4	SHOTIN	input to chip from selected one-shot
J5	IN8	data input
J6	IN6	data input

Pin number	Name	Function
J7	IN4	data input
J8	IN2	data input
J9	IN0	data input
J10		none
K1	SMOUT	three delay one-shot output
K2	MCA	master clock
K3	SHOTOUT	five delay one-shot output
K4	IN10	data input
K5	IN9	data input
K6	IN7	data input
K7	IN5	data input
K8	IN3	data input
K9	IN1	data input
K10	GND	pad ring ground

Table 4. 2DHIST Pinout

B. JUMPER HOOKUP FOR TESTING

Table 5 lists the jumpers which are required to be installed so that the 2DHIST is properly stimulated. Some variation is allowed with the one-shot input, pin J4. Three one-shots were fabricated on the 2DHIST chip to determine which would produce the best signal. The one-shots differ by the number of delay stages: 3, 5 or 7.

Pin 1	Pin 2	Signals
E2	E1	S0OUT-S0in
D1	D2	S1OUT-S1in
C1	B1	S2OUT-S2in
A2	B3	S3OUT-S3in
F1	K2	MC-MCA
F2	J3	SC-SCA
H1	H2	CLEAROUT-CLEARIN
A1	B2	MUXENOUT-MUXENIN
K3	J4	SHOTOUT-SHOTIN

Table 5. Jumpers for Testing the 2DHIST Chip

APPENDIX C. LOGIC ANALYZER WAVEFORMS

This appendix contains more waveforms from 2DHIST chip testing done on the HP16500B Logic Analyzer. It is worth noting that the waveforms for chip 6 on Figure 16 show narrow pulses on the signal line, SHOT 3. This is the three stage delay one-shot device. The one-shot, although producing narrow pulses, is doing so in an irregular pattern as evidenced by the uneven spacing between the three pulses. Figure 17 shows a closer look at the left most one-shot pulse emitted from chip 6. It was designed to have a pulse width of 3 ns. The measured width was 16.02 μ s. These are among the inconsistencies that lead us to conclude the chip was improperly fabricated.

Figure 18 represents the waveforms from chip 7. Other than the externally supplied clock pulses, MCA and SCA, all signal lines are constant. This is typical of eight of the twelve 2DHIST chips.

Chip 11 was interesting because of the irregularity of its waveforms. Figures 19 and 20 both came from the same chip however, the logic analyzer had different sec/Div settings to best show the waveforms.

Figure 20 shows the waveforms recorded from chip 12. It has most signal lines showing some activity but the one-shots never generate pulses.

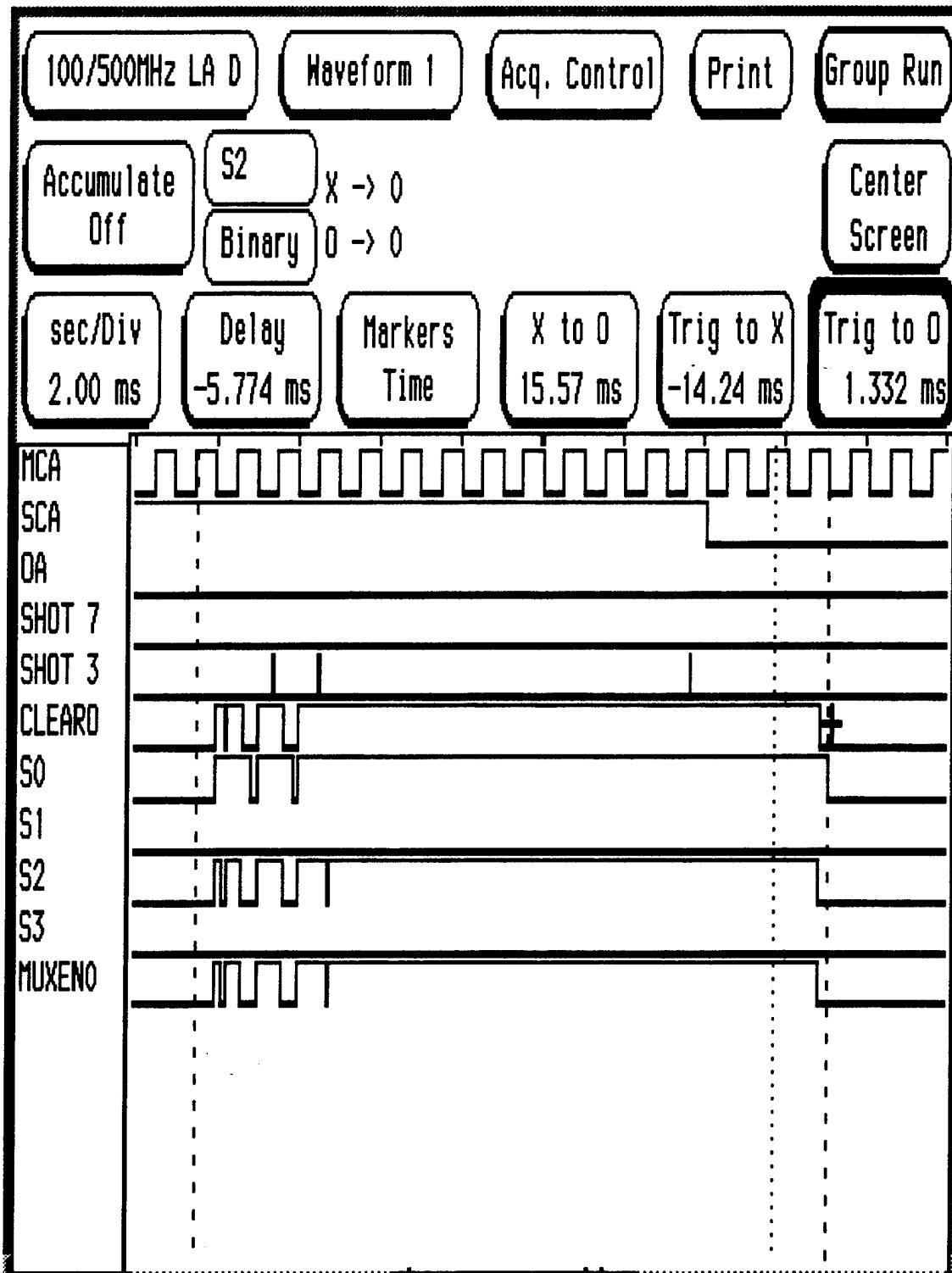


Figure 16. Chip 6 Waveforms

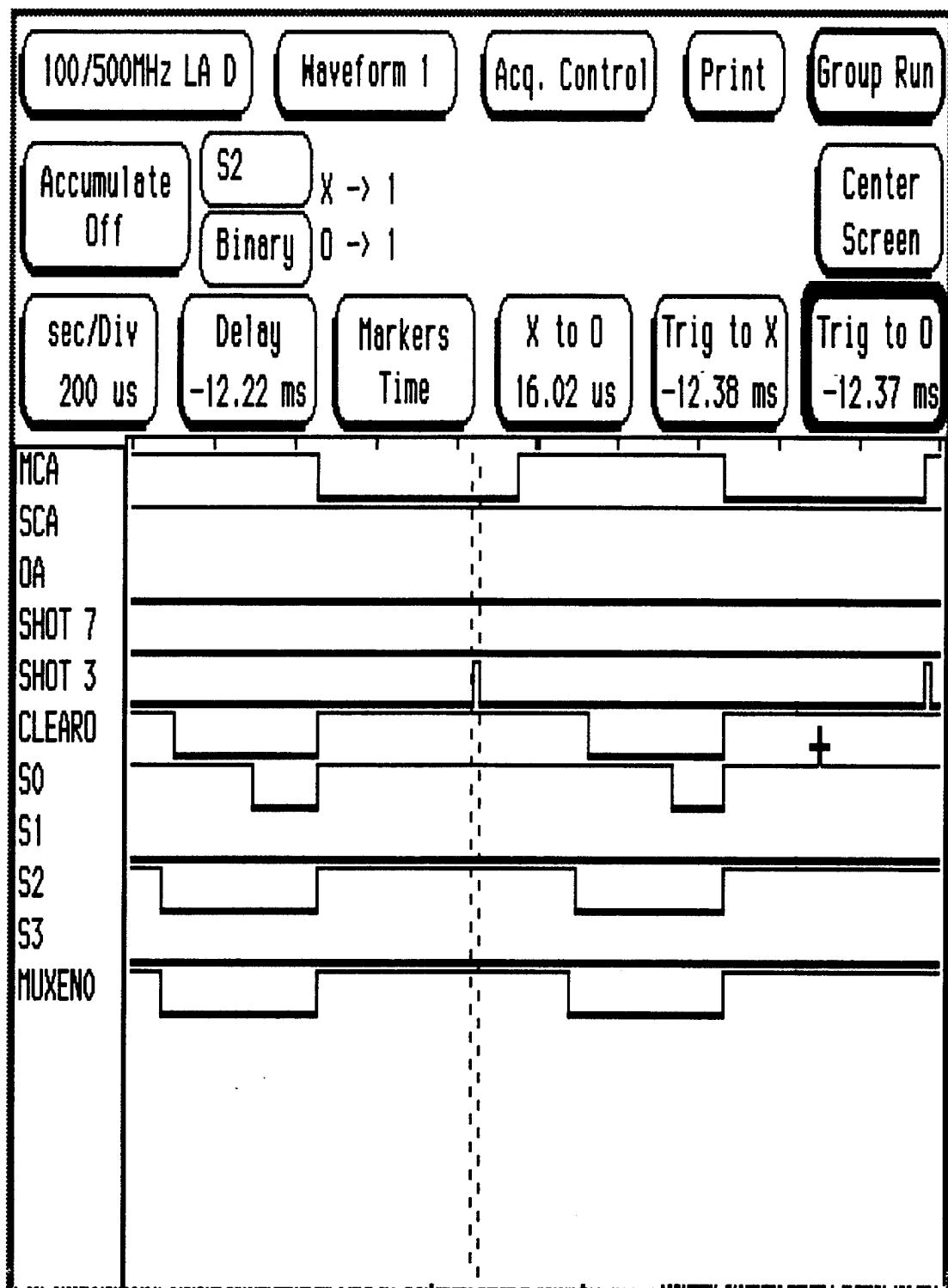


Figure 17. Chip 6 Waveforms, One-Shot Pulse

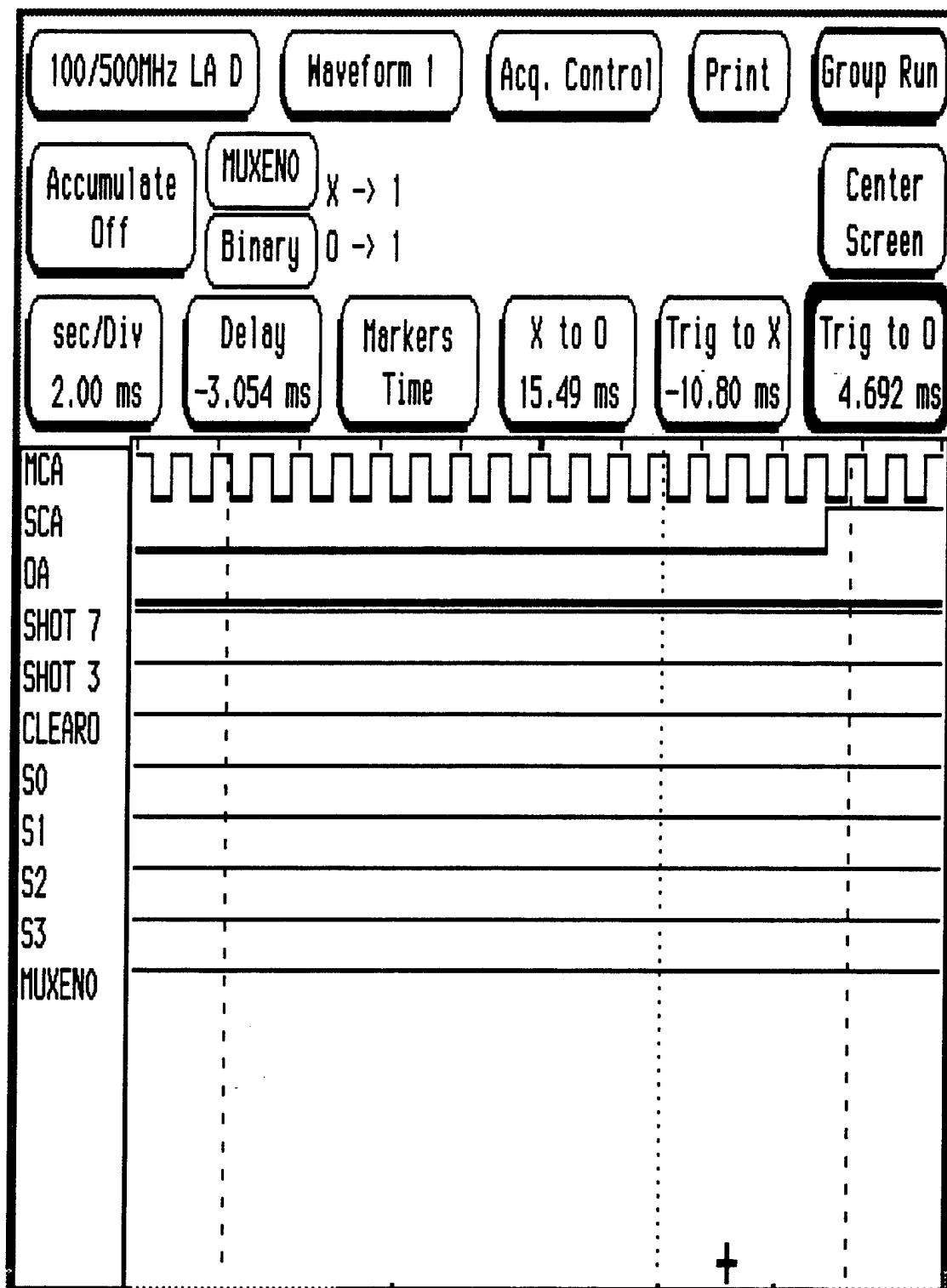


Figure 18. Chip 7 Waveforms

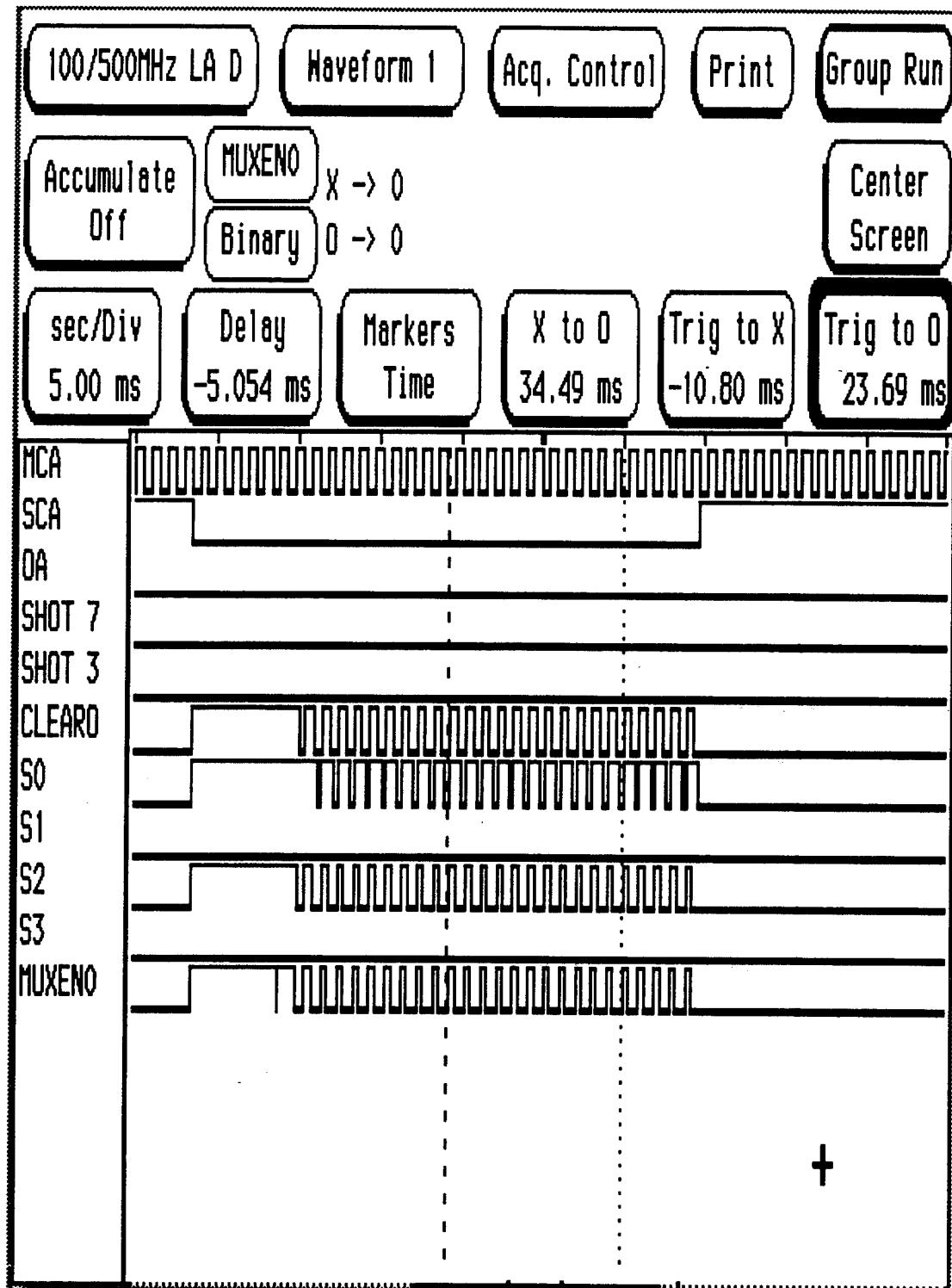


Figure 19. Chip 11 Waveforms, Part 1

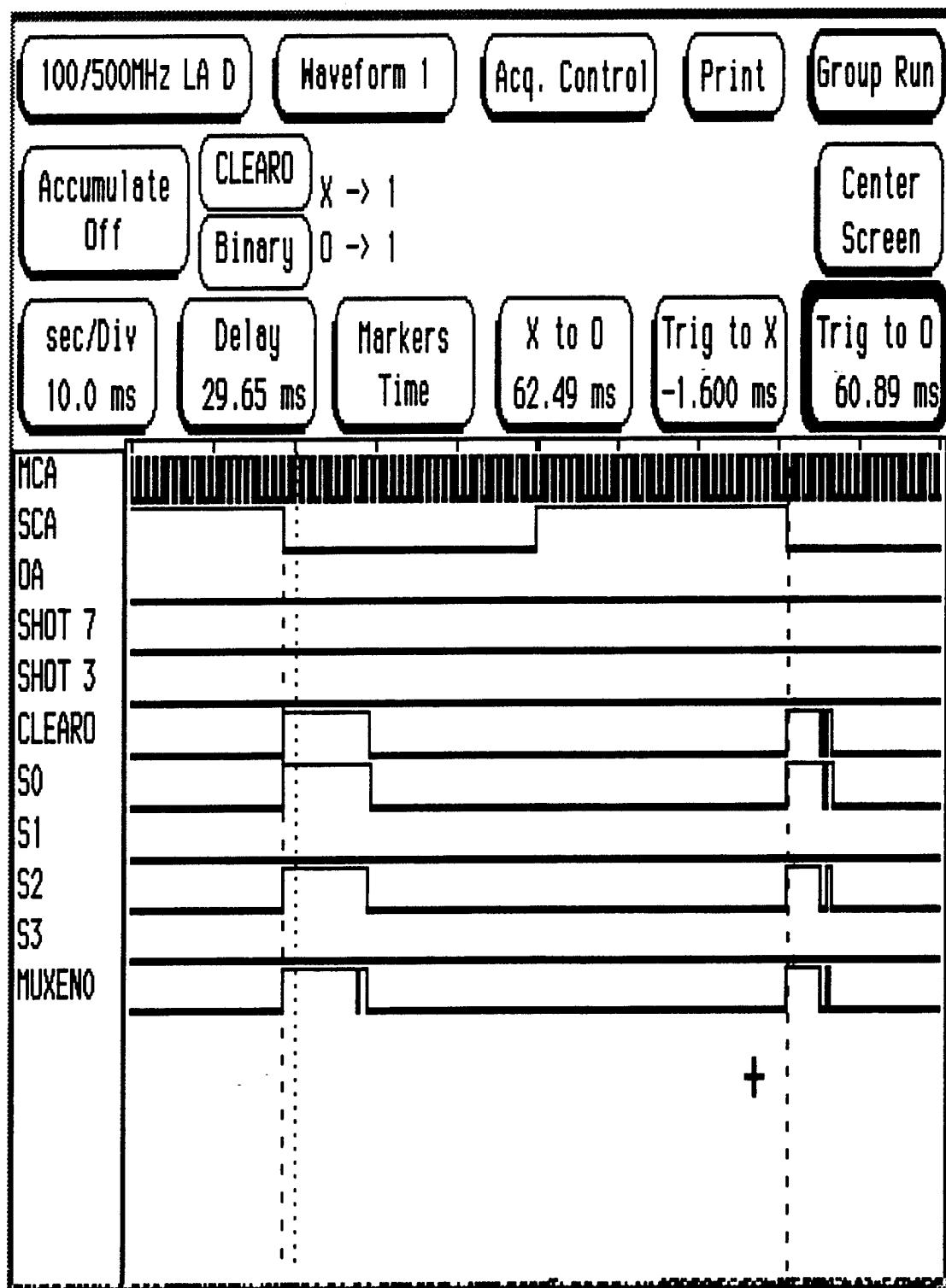


Figure 20. Chip 11 Waveforms, Part 2

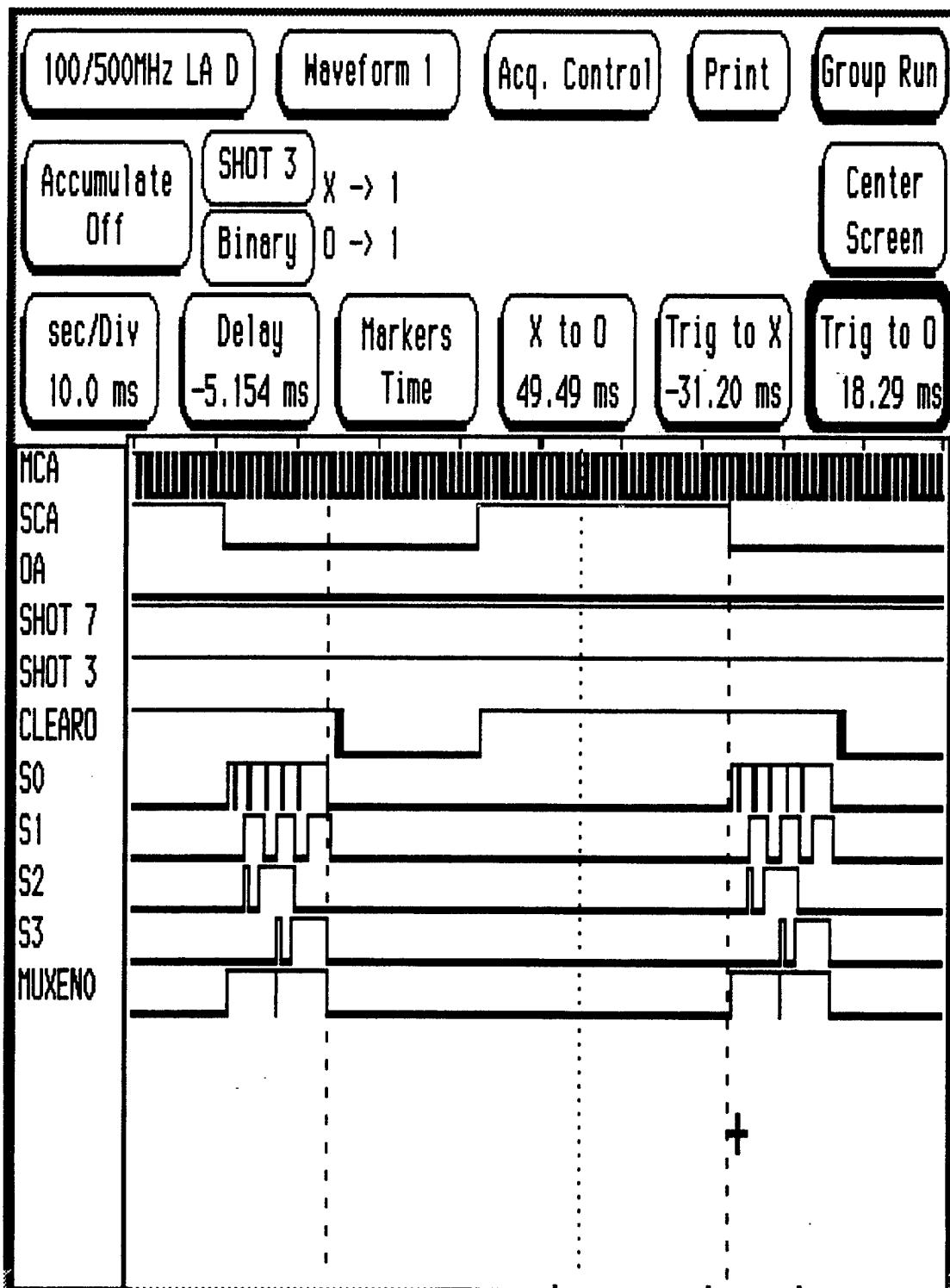


Figure 21. Chip 12 Waveforms

APPENDIX D. MATLAB CODE FOR LATCHUP TESTS

A. LATCH.M FILE

```
% this is 2DHIST current/voltage data to check for latchup
% written 2-2-95 by Pete Reinagel
% this program was run in MATLAB 4.2 on a SUN workstation
% filename is \reinagel\chip\data\latch.m
% variables: I is current readings in mA, V is voltage in 1/10 volt steps
clear
clf % clear any previous figure
% current readings data for 2DHIST chip # 1
I=[3.14 3.19 3.24 3.28 3.37 3.51 3.83 4.4 5.16 6.13 7.12 8.31 9.57 10.82 12.56
14.9 17.46 19.5 21.51 23.61 25.8 28.5 30.71 32.98 34.16 35.82 37.93 39.99 42.2 44.51
46.63 48.83 50.94 53.22 55.3 57.56 59.76 62.14 64.31 66.8 69.01 71.5 73.97 76.25
78.48 81. 83.22 85.65 87.97 90.43];
V=[0.1 :0.1: 5.0 ]; % voltage range is 0.1 volts to 5.0 volts
f1 = figure('PaperUnits','Inches','PaperPosition',[1.25 1.5 6 8.5]);
subplot(2,1,1)
plot(V, I)
grid
title('Latchup Test for 2DHIST chip ISI N44N CB2 #1')
xlabel('Voltage'), ylabel('Current (mA)')

% next is data for chip #2
I2 = [ 3.15 3.2 3.25 3.3 3.37 3.5 3.82 4.4 5.15 6.06 7.1 8.25 9.52 10.82 12.42
14.7 17.17 19.42 21.46 23.52 25.77 28.05 31.46 33.25 34.5 36.07 38.23 40.54 42.67
44.96 47.26 49.59 51.91 54.38 56.56 58.92 61.3 63.97 66.13 68.44 71.1 73.5 76.05
78.57 81.15 83.68 86.05 88.88 91.25 93.85 ];
```

```

subplot(2,1,2)
plot(V,I2)
grid
title('Latchup Test for 2DHIST chip ISI N44N CB2 #2')
xlabel('Voltage'), ylabel('Current (mA)')
print -Ppr14 latch1-2

% next is data for chip #3
I3 = [ 3.15 3.2 3.25 3.3 3.38 3.52 3.86 4.4 5.17 6.13 7.12 8.32 9.62 10.9 12.45
14.9 17.25 19.5 21.65 23.69 25.9 28.2 30.94 33.28 34.53 36.04 38.1 40.2 42.34 44.55
46.72 49.07 51.4 53.65 56.19 58.32 60.56 63.1 65.4 67.76 70.22 72.79 74.98 77.64 80.1
82.89 85.62 88.22 90.7 93.15 ];
subplot(2,1,1)
plot(V,I2)
grid
title('Latchup Test for 2DHIST chip ISI N44N CB2 #3')
xlabel('Voltage'), ylabel('Current (mA)')

% plot all three current vs. voltage curves on a single graph
subplot(2,1,2)
plot(V, I, V, I2, V, I3)
grid
title('Latchup Test for 2DHIST chips ISI N44N CB2 #1 #2 #3')
xlabel('Voltage')
ylabel('Current (mA)')
print -Ppr14 latchall

```

APPENDIX E. SIMULATION DATA

This appendix has the Pspice files used to simulate the 1DHIST chip. This code was archived on magnetic tape by the network operator for the ECE Department. At this time it is unknown what file name it will be archived under, but most likely REINAGEL or RICHSTEIN. It is being saved for further testing of the 1DHIST chip.

Files listed here include:

2hist.net	the netlist
2hist.als	the alias file
2hist.cir	the circuit file

The I/O error message on the last page is indicative of problems caused by Pspice 5.0a. The system on which the simulation was running before it terminated itself, has a 920 Mb hard disk drive that was only 60% full at that time. This was more than adequate to hold the 8 Mb data file being generated and any temporary files Pspice may have produced.

```
**** 03/21/95 10:54:15 ***** PSpice 5.0a (Sep 1991) ***** ID# 69325 ****
```

```
* Schematics Circuit File *
```

```
***** CIRCUIT DESCRIPTION
```

```
*****
```

```
.INC "/home3a/reinagel/ec3840/2hist.net"
```

```
**** INCLUDING /home3a/reinagel/ec3840/2hist.net ****
```

```
* Schematics Netlist *
```

```
X_U1 Photo_Detector $N_0092 +12Vdc -12Vdc $N_0092 LF356/LT
X_U2 Photo_Detector $N_0097 +12Vdc -12Vdc $N_0096 LF347/TI
R_R1 0 $N_0097 2.2M
R_R2 $N_0100 $N_0099 4.7k
R_R3 $N_0102 $N_0101 1k
R_R4 $N_0103 $N_0102 1k
C_C1 0 $N_0097 0.66uF
X_U3 $N_0101 $N_0092 +12Vdc -12Vdc $N_0100 LM324
D_D1 $N_0099 Vdd MR2510M
D_D2 0 $N_0099 MR2510M
D_D3 $N_0097 $N_0096 FJT1100
X_U4 $N_0097 $N_0103 +12Vdc -12Vdc $N_0103 LF347/TI
X_U5 Vdd $N_0099 $N_0110 $G_DPWR $G_DGND 74LS86A PARAMS:
```

```

+ IO_LEVEL=0 MNTYMXDLY=0
X_U6 $N_0113 $N_0110 CTR-0 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U8 $D_HI $D_LO $N_0124 $N_0113 . $G_DPWR $G_DGND 74LS123 PARAMS:
+ PULSE=50us IO_LEVEL=0 MNTYMXDLY=0
X_U9 SC MC $N_0124 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
v_V1 0 $N_0130 dc 12
X_U11 Photo_Detector $N_0134 +12Vdc -12Vdc $N_0133 LF347/TI
R_R9 $N_0130 $N_0134 2.2M
C_C2 0 $N_0134 0.66uF
D_D4 $N_0134 $N_0133 FJT1100
X_U12 $N_0134 $N_0138 +12Vdc -12Vdc $N_0138 LF347/TI
R_R10 $N_0139 $N_0102 1k
R_R11 $N_0141 $N_0140 4.7k
R_R12 $N_0139 $N_0142 1k
X_U16 $N_0142 $N_0092 +12Vdc -12Vdc $N_0141 LM324
D_D5 $N_0140 Vdd MR2510M
D_D6 0 $N_0140 MR2510M
X_U17 $N_0099 $N_0140 $N_0147 $G_DPWR $G_DGND 74LS86A PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U18 $N_0113 $N_0147 CTR-1 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R13 $N_0153 $N_0139 1k
R_R14 $N_0155 $N_0154 4.7k
R_R15 $N_0153 $N_0156 1k
X_U20 $N_0156 $N_0092 +12Vdc -12Vdc $N_0155 LM324
D_D7 $N_0154 Vdd MR2510M
D_D8 0 $N_0154 MR2510M
X_U21 $N_0140 $N_0154 $N_0161 $G_DPWR $G_DGND 74LS86A PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U22 $N_0113 $N_0161 CTR-2 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R16 $N_0167 $N_0153 1k
R_R17 $N_0169 $N_0168 4.7k
R_R18 $N_0167 $N_0170 1k
X_U23 $N_0170 $N_0092 +12Vdc -12Vdc $N_0169 LM324
D_D9 $N_0168 Vdd MR2510M
D_D10 0 $N_0168 MR2510M
X_U24 $N_0154 $N_0168 $N_0175 $G_DPWR $G_DGND 74LS86A PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U25 $N_0113 $N_0175 CTR-3 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R19 $N_0181 $N_0167 1k
R_R20 $N_0183 $N_0182 4.7k
R_R21 $N_0181 $N_0184 1k
X_U26 $N_0184 $N_0092 +12Vdc -12Vdc $N_0183 LM324
D_D11 $N_0182 Vdd MR2510M
D_D12 0 $N_0182 MR2510M
X_U27 $N_0168 $N_0182 $N_0189 $G_DPWR $G_DGND 74LS86A PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U28 $N_0113 $N_0189 CTR-4 $G_DPWR $G_DGND 74LS08 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R22 $N_0195 $N_0181 1k

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R_R23 \$N_0197 \$N_0196 4.7k
 R_R24 \$N_0195 \$N_0198 1k
 X_U29 \$N_0198 \$N_0092 +12Vdc -12Vdc \$N_0197 LM324
 D_D13 \$N_0196 Vdd MR2510M
 D_D14 0 \$N_0196 MR2510M
 X_U30 \$N_0182 \$N_0196 \$N_0203 \$G_DPWR \$G_DGND 74LS86A PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U31 \$N_0113 \$N_0203 CTR-5 \$G_DPWR \$G_DGND 74LS08 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 R_R25 \$N_0209 \$N_0195 1k
 R_R26 \$N_0211 \$N_0210 4.7k
 R_R27 \$N_0209 \$N_0212 1k
 X_U32 \$N_0212 \$N_0092 +12Vdc -12Vdc \$N_0211 LM324
 D_D15 \$N_0210 Vdd MR2510M
 D_D16 0 \$N_0210 MR2510M
 X_U33 \$N_0196 \$N_0210 \$N_0217 \$G_DPWR \$G_DGND 74LS86A PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U34 \$N_0113 \$N_0217 CTR-6 \$G_DPWR \$G_DGND 74LS08 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 R_R28 \$N_0138 \$N_0209 1k
 X_U35 \$N_0210 0 \$N_0224 \$G_DPWR \$G_DGND 74LS86A PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U36 \$N_0113 \$N_0224 CTR-7 \$G_DPWR \$G_DGND 74LS08 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 R_R5 \$N_0231 \$N_0230 100k
 R_R6 \$N_0232 \$N_0230 47k
 R_R7 \$N_0230 0 100k
 X_U10 \$N_0237 \$N_0238 +12Vdc -12Vdc Oscope LF356/LT
 R_R8 Oscope \$N_0238 47k
 X_U15 SC S3 muxen \$G_DPWR \$G_DGND 7432 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U19 muxen S0 S1 S2 0A 1A 2A 3A 4A 5A 6A 7A \$N_0231 . \$G_DPWR \$G_DGND 74LS251
 + PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U37 CTR-1 reset 1A 1B 1C 1D \$G_DPWR \$G_DGND 74LS393 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 R_R29 \$N_0267 \$N_0232 100k
 R_R30 \$N_0268 \$N_0232 47k
 X_U38 \$N_0271 reset 1E 1F 1G 1H \$G_DPWR \$G_DGND 74LS393 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U39 1D \$N_0271 \$G_DPWR \$G_DGND 7404 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U41 muxen S0 S1 S2 0B 1B 2B 3B 4B 5B 6B 7B \$N_0267 . \$G_DPWR \$G_DGND 74LS251
 + PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U42 CTR-2 reset 2A 2B 2C 2D \$G_DPWR \$G_DGND 74LS393 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 R_R31 \$N_0302 \$N_0268 100k
 R_R32 \$N_0303 \$N_0268 47k
 X_U43 \$N_0306 reset 2E 2F 2G 2H \$G_DPWR \$G_DGND 74LS393 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U44 2D \$N_0306 \$G_DPWR \$G_DGND 7404 PARAMS:
 + IO_LEVEL=0 MNTYMXDLY=0
 X_U46 muxen S0 S1 S2 0C 1C 2C 3C 4C 5C 6C 7C \$N_0302 . \$G_DPWR \$G_DGND 74LS251

```

+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U47 CTR-3 reset 3A 3B 3C 3D $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R33 $N_0337 $N_0303 100k
R_R34 $N_0338 $N_0303 47k
X_U48 $N_0341 reset 3E 3F 3G 3H $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U49 3D $N_0341 $G_DPWR $G_DGND 7404 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U51 muxen S0 S1 S2 0D 1D 2D 3D 4D 5D 6D 7D $N_0337 . $G_DPWR $G_DGND 74LS251
+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U52 CTR-4 reset 4A 4B 4C 4D $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R35 $N_0372 $N_0338 100k
R_R36 $N_0373 $N_0338 47k
X_U53 $N_0376 reset 4E 4F 4G 4H $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U54 4D $N_0376 $G_DPWR $G_DGND 7404 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U56 muxen S0 S1 S2 0E 1E 2E 3E 4E 5E 6E 7E $N_0372 . $G_DPWR $G_DGND 74LS251
+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U57 CTR-5 reset 5A 5B 5C 5D $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R37 $N_0407 $N_0373 100k
R_R38 $N_0408 $N_0373 47k
X_U58 $N_0411 reset 5E 5F 5G 5H $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U59 5D $N_0411 $G_DPWR $G_DGND 7404 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U61 muxen S0 S1 S2 0F 1F 2F 3F 4F 5F 6F 7F $N_0407 . $G_DPWR $G_DGND 74LS251
+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U62 CTR-6 reset 6A 6B 6C 6D $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R39 $N_0442 $N_0408 100k
R_R40 $N_0443 $N_0408 47k
X_U63 $N_0446 reset 6E 6F 6G 6H $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U64 6D $N_0446 $G_DPWR $G_DGND 7404 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U66 muxen S0 S1 S2 0G 1G 2G 3G 4G 5G 6G 7G $N_0442 . $G_DPWR $G_DGND 74LS251
+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U67 CTR-7 reset 7A 7B 7C 7D $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
R_R41 $N_0477 $N_0443 100k
R_R42 $N_0237 $N_0443 47k
X_U68 $N_0480 reset 7E 7F 7G 7H $G_DPWR $G_DGND 74LS393 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U69 7D $N_0480 $G_DPWR $G_DGND 7404 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0

```

```

X_U71 muxen S0 S1 S2 0H 1H 2H 3H 4H 5H 6H 7H $N_0477 . $G_DPWR $G_DGND 74LS251
+ PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
X_U72 $D_HI $D_LO SC reset . $G_DPWR $G_DGND 74LS123 PARAMS:
+ PULSE=50us IO_LEVEL=0 MNTYMXDLY=0
V_V5 $N_0517 0
+PULSE 0 5 0 5ns 10ns .5ms 1.02ms
V_V6 $N_0519 0
+PULSE 0 5 0 5ns 10ns 16.38ms 32.77ms
V_V7 $N_0520 0
+PULSE 0 5 0 5ns 10ns 32.77ms 65.54ms
X_U73 $N_0519 PC $G_DPWR $G_DGND delay PARAMS:
+ DELAY=1ns TOL=10 IO_LEVEL=0 MNTYMXDLY=0
X_U74 $N_0520 SC $G_DPWR $G_DGND delay PARAMS:
+ DELAY=1ns TOL=10 IO_LEVEL=0 MNTYMXDLY=0
X_U75 MC $D_HI S3 $D_HI $D_NC $D_NC $D_NC $D_NC S0 S1 S2 S3 $D_NC $D_NC $G_DPWR
+ $G_DGND 74LS193 PARAMS:
+ IO_LEVEL=0 MNTYMXDLY=0
V_V8 S3 0
+PWL 0 5 200ns 5 205ns 0
X_U76 $N_0517 MC $G_DPWR $G_DGND delay PARAMS:
+ DELAY=1ns TOL=10 IO_LEVEL=0 MNTYMXDLY=0
v_V2 -12Vdc 0 dc -12
v_V3 +12Vdc 0 dc 12
v_V4 Vdd 0 5
V_V10 Photo_Detector 0
+PULSE 0 5 0 5ns 10ns 16.38ms 32.77ms

```

***** RESUMING /home3a/reinagel/ec3840/2hist.cir *****
 .INC "/home3a/reinagel/ec3840/2hist.als"

***** INCLUDING /home3a/reinagel/ec3840/2hist.als *****
 * Schematics Aliases *

.ALIASES

```

X_U1 U1(+=Photo_Detector -$N_0092 3=+12Vdc 4=-12Vdc 5=$N_0092 )
X_U2 U2(+=Photo_Detector -$N_0097 3=+12Vdc 4=-12Vdc 5=$N_0096 )
R_R1 R1(1=0 2=$N_0097 )
R_R2 R2(1=$N_0100 2=$N_0099 )
R_R3 R3(1=$N_0102 2=$N_0101 )
R_R4 R4(1=$N_0103 2=$N_0102 )
C_C1 C1(1=0 2=$N_0097 )
X_U3 U3(+$N_0101 -$N_0092 3=+12Vdc 4=-12Vdc 5=$N_0100 )
D_D1 D1(1=$N_0099 2=Vdd )

```

D_D2 D2(1=0 2=\$N_0099)
 D_D3 D3(1=\$N_0097 2=\$N_0096)
 X_U4 U4(+=\$N_0097 -\$N_0103 3=+12Vdc 4=-12Vdc 5=\$N_0103)
 X_U5 U5(A=Vdd B=\$N_0099 Y=\$N_0110 PWR=\$G_DPWR GND=\$G_DGND)
 X_U6 U6(A=\$N_0113 B=\$N_0110 Y=CTR-0 PWR=\$G_DPWR GND=\$G_DGND)
 X_U8 U8(CLRbar=\$D_HI A=\$D_LO B=\$N_0124 Q=\$N_0113 Qbar=. PWR=\$G_DPWR GND=\$G_DGND +)
 X_U9 U9(A=SC B=MC Y=\$N_0124 PWR=\$G_DPWR GND=\$G_DGND).
 v_V1 V1(+=\$N_0130)
 X_U11 U11(+=Photo_Detector -\$N_0134 3=+12Vdc 4=-12Vdc 5=\$N_0133)
 R_R9 R9(1=\$N_0130 2=\$N_0134)
 C_C2 C2(1=0 2=\$N_0134)
 D_D4 D4(1=\$N_0134 2=\$N_0133)
 X_U12 U12(+=\$N_0134 -\$N_0138 3=+12Vdc 4=-12Vdc 5=\$N_0138)
 R_R10 R10(1=\$N_0139 2=\$N_0102)
 R_R11 R11(1=\$N_0141 2=\$N_0140)
 R_R12 R12(1=\$N_0139 2=\$N_0142)
 X_U16 U16(+=\$N_0142 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0141)
 D_D5 D5(1=\$N_0140 2=Vdd)
 D_D6 D6(1=0 2=\$N_0140)
 X_U17 U17(A=\$N_0099 B=\$N_0140 Y=\$N_0147 PWR=\$G_DPWR GND=\$G_DGND)
 X_U18 U18(A=\$N_0113 B=\$N_0147 Y=CTR-1 PWR=\$G_DPWR GND=\$G_DGND)
 R_R13 R13(1=\$N_0153 2=\$N_0139)
 R_R14 R14(1=\$N_0155 2=\$N_0154)
 R_R15 R15(1=\$N_0153 2=\$N_0156)
 X_U20 U20(+=\$N_0156 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0155)
 D_D7 D7(1=\$N_0154 2=Vdd)
 D_D8 D8(1=0 2=\$N_0154)

X_U21 U21(A=\$N_0140 B=\$N_0154 Y=\$N_0161 PWR=\$G_DPWR GND=\$G_DGND)
X_U22 U22(A=\$N_0113 B=\$N_0161 Y=CTR-2 PWR=\$G_DPWR GND=\$G_DGND)
R_R16 R16(1=\$N_0167 2=\$N_0153)
R_R17 R17(1=\$N_0169 2=\$N_0168)
R_R18 R18(1=\$N_0167 2=\$N_0170)
X_U23 U23(+=\$N_0170 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0169)
D_D9 D9(1=\$N_0168 2=Vdd)
D_D10 D10(1=0 2=\$N_0168)
X_U24 U24(A=\$N_0154 B=\$N_0168 Y=\$N_0175 PWR=\$G_DPWR GND=\$G_DGND)
X_U25 U25(A=\$N_0113 B=\$N_0175 Y=CTR-3 PWR=\$G_DPWR GND=\$G_DGND)
R_R19 R19(1=\$N_0181 2=\$N_0167)
R_R20 R20(1=\$N_0183 2=\$N_0182)
R_R21 R21(1=\$N_0181 2=\$N_0184)
X_U26 U26(+=\$N_0184 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0183)
D_D11 D11(1=\$N_0182 2=Vdd)
D_D12 D12(1=0 2=\$N_0182)
X_U27 U27(A=\$N_0168 B=\$N_0182 Y=\$N_0189 PWR=\$G_DPWR GND=\$G_DGND)
X_U28 U28(A=\$N_0113 B=\$N_0189 Y=CTR-4 PWR=\$G_DPWR GND=\$G_DGND)
R_R22 R22(1=\$N_0195 2=\$N_0181)
R_R23 R23(1=\$N_0197 2=\$N_0196)
R_R24 R24(1=\$N_0195 2=\$N_0198)
X_U29 U29(+=\$N_0198 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0197)
D_D13 D13(1=\$N_0196 2=Vdd)
D_D14 D14(1=0 2=\$N_0196)
X_U30 U30(A=\$N_0182 B=\$N_0196 Y=\$N_0203 PWR=\$G_DPWR GND=\$G_DGND)
X_U31 U31(A=\$N_0113 B=\$N_0203 Y=CTR-5 PWR=\$G_DPWR GND=\$G_DGND)
R_R25 R25(1=\$N_0209 2=\$N_0195)

R_R26 R26(1=\$N_0211 2=\$N_0210)
 R_R27 R27(1=\$N_0209 2=\$N_0212)
 X_U32 U32(+=\$N_0212 -\$N_0092 3=+12Vdc 4=-12Vdc 5=\$N_0211)
 D_D15 D15(1=\$N_0210 2=Vdd)
 D_D16 D16(1=0 2=\$N_0210)
 X_U33 U33(A=\$N_0196 B=\$N_0210 Y=\$N_0217 PWR=\$G_DPWR GND=\$G_DGND)
 X_U34 U34(A=\$N_0113 B=\$N_0217 Y=CTR-6 PWR=\$G_DPWR GND=\$G_DGND)
 R_R28 R28(1=\$N_0138 2=\$N_0209)
 X_U35 U35(A=\$N_0210 B=0 Y=\$N_0224 PWR=\$G_DPWR GND=\$G_DGND)
 X_U36 U36(A=\$N_0113 B=\$N_0224 Y=CTR-7 PWR=\$G_DPWR GND=\$G_DGND)
 R_R5 R5(1=\$N_0231 2=\$N_0230)
 R_R6 R6(1=\$N_0232 2=\$N_0230)
 R_R7 R7(1=\$N_0230 2=0)
 X_U10 U10(+=\$N_0237 -\$N_0238 3=+12Vdc 4=-12Vdc 5=Oscope)
 R_R8 R8(1=Oscope 2=\$N_0238)
 X_U15 U15(A=SC B=S3 Y=muxen PWR=\$G_DPWR GND=\$G_DGND)
 X_U19 U19(Gbar=muxen A=S0 B=S1 C=S2 D0=0A D1=1A D2=2A D3=3A D4=4A D5=5A D6=6A
 + D7=7A Y=\$N_0231 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)
 X_U37 U37(A=CTR-1 CLR=reset QA=1A QB=1B QC=1C QD=1D PWR=\$G_DPWR GND=\$G_DGND
 +)
 R_R29 R29(1=\$N_0267 2=\$N_0232)
 R_R30 R30(1=\$N_0268 2=\$N_0232)
 X_U38 U38(A=\$N_0271 CLR=reset QA=1E QB=1F QC=1G QD=1H PWR=\$G_DPWR GND=\$G_DGND
 +)
 X_U39 U39(A=1D Y=\$N_0271 PWR=\$G_DPWR GND=\$G_DGND)
 X_U41 U41(Gbar=muxen A=S0 B=S1 C=S2 D0=0B D1=1B D2=2B D3=3B D4=4B D5=5B D6=6B
 + D7=7B Y=\$N_0267 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)
 X_U42 U42(A=CTR-2 CLR=reset QA=2A QB=2B QC=2C QD=2D PWR=\$G_DPWR GND=\$G_DGND
 +)

R_R31 R31(1=\$N_0302 2=\$N_0268)

R_R32 R32(1=\$N_0303 2=\$N_0268)

X_U43 U43(A=\$N_0306 CLR=reset QA=2E QB=2F QC=2G QD=2H PWR=\$G_DPWR GND=\$G_DGND
+)

X_U44 U44(A=2D Y=\$N_0306 PWR=\$G_DPWR GND=\$G_DGND)

X_U46 U46(Gbar=muxen A=S0 B=S1 C=S2 D0=0C D1=1C D2=2C D3=3C D4=4C D5=5C D6=6C
+ D7=7C Y=\$N_0302 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

X_U47 U47(A=CTR-3 CLR=reset QA=3A QB=3B QC=3C QD=3D PWR=\$G_DPWR GND=\$G_DGND
+)

R_R33 R33(1=\$N_0337 2=\$N_0303)

R_R34 R34(1=\$N_0338 2=\$N_0303)

X_U48 U48(A=\$N_0341 CLR=reset QA=3E QB=3F QC=3G QD=3H PWR=\$G_DPWR GND=\$G_DGND
+)

X_U49 U49(A=3D Y=\$N_0341 PWR=\$G_DPWR GND=\$G_DGND)

X_U51 U51(Gbar=muxen A=S0 B=S1 C=S2 D0=0D D1=1D D2=2D D3=3D D4=4D D5=5D D6=6D
+ D7=7D Y=\$N_0337 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

X_U52 U52(A=CTR-4 CLR=reset QA=4A QB=4B QC=4C QD=4D PWR=\$G_DPWR GND=\$G_DGND
+)

R_R35 R35(1=\$N_0372 2=\$N_0338)

R_R36 R36(1=\$N_0373 2=\$N_0338)

X_U53 U53(A=\$N_0376 CLR=reset QA=4E QB=4F QC=4G QD=4H PWR=\$G_DPWR GND=\$G_DGND
+)

X_U54 U54(A=4D Y=\$N_0376 PWR=\$G_DPWR GND=\$G_DGND)

X_U56 U56(Gbar=muxen A=S0 B=S1 C=S2 D0=0E D1=1E D2=2E D3=3E D4=4E D5=5E D6=6E
+ D7=7E Y=\$N_0372 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

X_U57 U57(A=CTR-5 CLR=reset QA=5A QB=5B QC=5C QD=5D PWR=\$G_DPWR GND=\$G_DGND
+)

R_R37 R37(1=\$N_0407 2=\$N_0373)

R_R38 R38(1=\$N_0408 2=\$N_0373)

X_U58 U58(A=\$N_0411 CLR=reset QA=5E QB=5F QC=5G QD=5H PWR=\$G_DPWR GND=\$G_DGND
+)

X_U59 U59(A=5D Y=\$N_0411 PWR=\$G_DPWR GND=\$G_DGND)

X_U61 U61(Gbar=muxen A=S0 B=S1 C=S2 D0=0F D1=1F D2=2F D3=3F D4=4F D5=5F D6=6F
 + D7=7F Y=\$N_0407 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

 X_U62 U62(A=CTR-6 CLR=reset QA=6A QB=6B QC=6C QD=6D PWR=\$G_DPWR GND=\$G_DGND
 +)

 R_R39 R39(1=\$N_0442 2=\$N_0408)

 R_R40 R40(1=\$N_0443 2=\$N_0408)

 X_U63 U63(A=\$N_0446 CLR=reset QA=6E QB=6F QC=6G QD=6H PWR=\$G_DPWR GND=\$G_DGND
 +)

 X_U64 U64(A=6D Y=\$N_0446 PWR=\$G_DPWR GND=\$G_DGND)

 X_U66 U66(Gbar=muxen A=S0 B=S1 C=S2 D0=0G D1=1G D2=2G D3=3G D4=4G D5=5G D6=6G
 + D7=7G Y=\$N_0442 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

 X_U67 U67(A=CTR-7 CLR=reset QA=7A QB=7B QC=7C QD=7D PWR=\$G_DPWR GND=\$G_DGND
 +)
 R_R41 R41(1=\$N_0477 2=\$N_0443)

 R_R42 R42(1=\$N_0237 2=\$N_0443)

 X_U68 U68(A=\$N_0480 CLR=reset QA=7E QB=7F QC=7G QD=7H PWR=\$G_DPWR GND=\$G_DGND
 +)

 X_U69 U69(A=7D Y=\$N_0480 PWR=\$G_DPWR GND=\$G_DGND)

 X_U71 U71(Gbar=muxen A=S0 B=S1 C=S2 D0=0H D1=1H D2=2H D3=3H D4=4H D5=5H D6=6H
 + D7=7H Y=\$N_0477 Wbar=. PWR=\$G_DPWR GND=\$G_DGND)

 X_U72 U72(CLrbar=\$D_HI A=\$D_LO B=SC Q=reset Qbar=. PWR=\$G_DPWR GND=\$G_DGND
 +)

 V_V5 V5(+=\$N_0517 --0)

 V_V6 V6(+=\$N_0519 --0)

 V_V7 V7(+=\$N_0520 --0)

 X_U73 U73(IN=\$N_0519 OUT=PC PWR=\$G_DPWR GND=\$G_DGND)

 X_U74 U74(IN=\$N_0520 OUT=SC PWR=\$G_DPWR GND=\$G_DGND)

 X_U75 U75(UP=MC DOWN=\$D_HI CLR=S3 LOADbar=\$D_HI A=\$D_NC B=\$D_NC C=\$D_NC D=\$D_NC
 + QA=S0 QB=S1 QC=S2 QD=S3 Bbar=\$D_NC Cbar=\$D_NC PWR=\$G_DPWR GND=\$G_DGND)

 V_V8 V8(+=\$S3 --0)

 X_U76 U76(IN=\$N_0517 OUT=MC PWR=\$G_DPWR GND=\$G_DGND)

 v_V2 V2(+=-12Vdc --0)

```

v_V3      V3(+=+12Vdc -=0 )
v_V4      V4(+=Vdd -=0 )
V_V10     V10(+=Photo_Detector -=0 )

```

```

- _(.=.)
- _($D_LO=$D_LO)
- _($D_HI=$D_HI)
- _(MC=MC)
- _(PC=PC)
- _(SC=SC)
- _($D_NC=$D_NC)
- _(_Photo_Detector=Photo_Detector)
.ENDALIASES

```

```

**** RESUMING /home3a/reinagel/ec3840/2hist.cir ****
.LIB "myparts.lib"

```

```

** Analysis setup **


```

```

.LIB
.tran 2us    2ms 400us 100ns
.SAVEBIAS "2histbias" TRAN
.LOADBIAS "2histbias"
.OPTIONS RELTOL=0.01
.OPTIONS ACCT

```

```

.END

```

```

**** Generated AtoD and DtoA Interfaces ****

```

```

*
* Analog/Digital interface for node 0
*
* Moving X_U35.UIBUF:IN2 from analog node 0 to new digital node 0$AtoD
X$0_AtoD1 0 0$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node S3
*
* Moving X_U75.U1:IN3 from analog node S3 to new digital node S3$AtoD
X$S3_AtoD1 S3 S3$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U15.U1:IN2 from analog node S3 to new digital node S3$AtoD2
X$S3_AtoD2 S3 S3$AtoD2 $G_DPWR $G_DGND AtoD_STD

```

```

+    PARAMS: CAPACITANCE= 0
* Moving X_U75.U16:OUT4 from analog node S3 to new digital node S3$DtoA
X$$S3_DtoA1 S3$DtoA S3 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
* Moving X_U75.U17:OUT4 from analog node S3 to new digital node S3$DtoA2
X$$S3_DtoA2 S3$DtoA2 S3 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
*
* Analog/Digital interface for node Vdd
*
* Moving X_U5.UIBUF:IN1 from analog node Vdd to new digital node Vdd$AtoD
X$Vdd_AtoD1 Vdd Vdd$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0099
*
* Moving X_U17.UIBUF:IN1 from analog node $N_0099 to new digital node $N_0099$AtoD
X$$N_0099_AtoD1 $N_0099 $N_0099$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U5.UIBUF:IN2 from analog node $N_0099 to new digital node $N_0099$AtoD2
X$$N_0099_AtoD2 $N_0099 $N_0099$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0140
*
* Moving X_U21.UIBUF:IN1 from analog node $N_0140 to new digital node $N_0140$AtoD
X$$N_0140_AtoD1 $N_0140 $N_0140$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U17.UIBUF:IN2 from analog node $N_0140 to new digital node $N_0140$AtoD2
X$$N_0140_AtoD2 $N_0140 $N_0140$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0154
*
* Moving X_U24.UIBUF:IN1 from analog node $N_0154 to new digital node $N_0154$AtoD
X$$N_0154_AtoD1 $N_0154 $N_0154$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U21.UIBUF:IN2 from analog node $N_0154 to new digital node $N_0154$AtoD2
X$$N_0154_AtoD2 $N_0154 $N_0154$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0168
*
* Moving X_U27.UIBUF:IN1 from analog node $N_0168 to new digital node $N_0168$AtoD
X$$N_0168_AtoD1 $N_0168 $N_0168$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U24.UIBUF:IN2 from analog node $N_0168 to new digital node $N_0168$AtoD2
X$$N_0168_AtoD2 $N_0168 $N_0168$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0182
*
* Moving X_U30.UIBUF:IN1 from analog node $N_0182 to new digital node $N_0182$AtoD
X$$N_0182_AtoD1 $N_0182 $N_0182$AtoD $G_DPWR $G_DGND AtoD_LS

```

```

+    PARAMS: CAPACITANCE= 0
* Moving X_U27.UIBUF:IN2 from analog node $N_0182 to new digital node $N_0182$AtoD2
X$$N_0182_AtoD2 $N_0182 $N_0182$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0196
*
* Moving X_U33.UIBUF:IN1 from analog node $N_0196 to new digital node $N_0196$AtoD
X$$N_0196_AtoD1 $N_0196 $N_0196$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U30.UIBUF:IN2 from analog node $N_0196 to new digital node $N_0196$AtoD2
X$$N_0196_AtoD2 $N_0196 $N_0196$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0210
*
* Moving X_U35.UIBUF:IN1 from analog node $N_0210 to new digital node $N_0210$AtoD
X$$N_0210_AtoD1 $N_0210 $N_0210$AtoD $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
* Moving X_U33.UIBUF:IN2 from analog node $N_0210 to new digital node $N_0210$AtoD2
X$$N_0210_AtoD2 $N_0210 $N_0210$AtoD2 $G_DPWR $G_DGND AtoD_LS
+    PARAMS: CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0231
*
* Moving X_U19.U5:OUT from analog node $N_0231 to new digital node $N_0231$DtoA
X$$N_0231_DtoA1 $N_0231$DtoA $N_0231 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0267
*
* Moving X_U41.U5:OUT from analog node $N_0267 to new digital node $N_0267$DtoA
X$$N_0267_DtoA1 $N_0267$DtoA $N_0267 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0302
*
* Moving X_U46.U5:OUT from analog node $N_0302 to new digital node $N_0302$DtoA
X$$N_0302_DtoA1 $N_0302$DtoA $N_0302 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0337
*
* Moving X_U51.U5:OUT from analog node $N_0337 to new digital node $N_0337$DtoA
X$$N_0337_DtoA1 $N_0337$DtoA $N_0337 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108  DRVL= 157  CAPACITANCE= 0
*
* Analog/Digital interface for node $N_0372
*
* Moving X_U56.U5:OUT from analog node $N_0372 to new digital node $N_0372$DtoA

```

```

X$$N_0372_DtoA1 $N_0372$DtoA $N_0372 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108   DRVL= 157   CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0407
*
* Moving X_U61.U5:OUT from analog node $N_0407 to new digital node $N_0407$DtoA

X$$N_0407_DtoA1 $N_0407$DtoA $N_0407 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108   DRVL= 157   CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0442
*
* Moving X_U66.U5:OUT from analog node $N_0442 to new digital node $N_0442$DtoA

X$$N_0442_DtoA1 $N_0442$DtoA $N_0442 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108   DRVL= 157   CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0477
*
* Moving X_U71.U5:OUT from analog node $N_0477 to new digital node $N_0477$DtoA

X$$N_0477_DtoA1 $N_0477$DtoA $N_0477 $G_DPWR $G_DGND DtoA_LS
+    PARAMS: DRVH= 108   DRVL= 157   CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0517
*
* Moving X_U76.U1:IN1 from analog node $N_0517 to new digital node $N_0517$AtoD

X$$N_0517_AtoD1 $N_0517 $N_0517$AtoD $G_DPWR $G_DGND AtoD_STD
+    PARAMS: CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0519
*
* Moving X_U73.U1:IN1 from analog node $N_0519 to new digital node $N_0519$AtoD

X$$N_0519_AtoD1 $N_0519 $N_0519$AtoD $G_DPWR $G_DGND AtoD_STD
+    PARAMS: CAPACITANCE=  0
*
* Analog/Digital interface for node $N_0520
*
* Moving X_U74.U1:IN1 from analog node $N_0520 to new digital node $N_0520$AtoD

X$$N_0520_AtoD1 $N_0520 $N_0520$AtoD $G_DPWR $G_DGND AtoD_STD
+    PARAMS: CAPACITANCE=  0
*
* Analog/Digital interface power supply subckt
*
X$DIGIFPWR 0 DIGIFPWR

.END ;(end of AtoD and DtoA interfaces)

```

**** EXPANSION OF SUBCIRCUIT X\$DIGIFPWR ****

X\$DIGIFPWR.VDPWR \$G_DPWR \$G_DGND X\$DIGIFPWR.VOLTAGE
X\$DIGIFPWR.R1 \$G_DPWR 0 1MEG
X\$DIGIFPWR.VDGND \$G_DGND 0 X\$DIGIFPWR.REFERENCE
X\$DIGIFPWR.R2 \$G_DGND 0 1MEG

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* Schematics Circuit File *

**** Diode MODEL PARAMETERS

FJT1100 MR2510M X_U1.dm1 X_U1.dm2
IS 24.320000E-21 639.200000E-15 1.000000E-15 800.000000E-18
ISR 290.000000E-12 4.623000E-06
IKF 6.473
BV 30 43.2
IBV 100.000000E-06
RS .1 1.833000E-03
TT 5.000000E-09 5.338000E-06
CJO 4.137000E-12 423.700000E-12
VJ .75 .75
M .3333 .4272

X_U1.dm3 X_U1.dm4 X_U2.dx X_U3.dx
IS 100.000000E-18 1.000000E-09 800.000000E-18 800.000000E-18
RS 1

X_U4.dx X_U11.dx X_U12.dx X_U16.dx
IS 800.000000E-18 800.000000E-18 800.000000E-18 800.000000E-18
RS 1

X_U20.dx X_U23.dx X_U26.dx X_U29.dx
IS 800.000000E-18 800.000000E-18 800.000000E-18 800.000000E-18
RS 1 1 1 1

X_U32.dx X_U10.dm1 X_U10.dm2 X_U10.dm3
IS 800.000000E-18 1.000000E-15 800.000000E-18 100.000000E-18
BV 43.2
RS 1

X_U10.dm4
IS 1.000000E-09

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**** BJT MODEL PARAMETERS

X_U3.qx	X_U16.qx	X_U20.qx	X_U23.qx
PNP	PNP	PNP	PNP
IS 800.000000E-18	800.000000E-18	800.000000E-18	800.000000E-18
BF 166.7	166.7	166.7	166.7
NF 1	1	1	1
BR 1	1	1	1
NR 1	1	1	1

X_U26.qx	X_U29.qx	X_U32.qx
PNP	PNP	PNP
IS 800.000000E-18	800.000000E-18	800.000000E-18
BF 166.7	166.7	166.7
NF 1	1	1
BR 1	1	1
NR 1	1	1

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**** Junction FET MODEL PARAMETERS

X_U1.jm1	X_U1.jm2	X_U2.jx	X_U4.jx
PJF	PJF	PJF	PJF
VTO -1	-.997	-1	-1
BETA 925.280000E-06	925.280000E-06	235.100000E-06	235.100000E-06
IS 31.500000E-12	28.500000E-12	25.000000E-12	25.000000E-12

X_U11.jx	X_U12.jx	X_U10.jm1	X_U10.jm2
PJF	PJF	PJF	PJF
VTO -1	-1	-1	-.997
BETA 235.100000E-06	235.100000E-06	925.280000E-06	925.280000E-06
IS 25.000000E-12	25.000000E-12	31.500000E-12	28.500000E-12

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**** Digital Input MODEL PARAMETERS

```
*****
DIN74LS
FILE DSO_DTOA
FORMAT 6
Timestep 100.000000E-12
S0NAME 0
S0TSW 5.000000E-09
S0RLO 29.6
S0RHI 1.450000E+03
S1NAME 1
S1TSW 4.500000E-09
S1RLO 172
S1RHI 73.9
S2NAME X
S2TSW 4.500000E-09
S2RLO 51.2
S2RHI 158
S3NAME R
S3TSW 4.500000E-09
S3RLO 51.2
S3RHI 158
S4NAME F
S4TSW 4.500000E-09
S4RLO 51.2
S4RHI 158
S5NAME Z
S5TSW 4.500000E-09
S5RLO 200.000000E+03
S5RHI 200.000000E+03
```

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* Schematics Circuit File *

**** Digital Output MODEL PARAMETERS

```
*****
DO74LS      DO74
FILE DSO_ATOD    DSO_ATOD
FORMAT 6       6
CHGONLY 1      1
Timestep 100.000000E-12 100.000000E-12
S0NAME X      X
S0VHI 2        2
S0VLO .8       .8
S1NAME 0      0
S1VHI .8       .8
S1VLO -1.5     -1.5
S2NAME R      R
S2VHI 1.27     1.4
S2VLO .8       .8
```

S3NAME	R	R
S3VHI	2	2
S3VLO	1.17	1.3
S4NAME	X	X
S4VHI	2	2
S4VLO	.8	.8
S5NAME	1	1
S5VHI	7	7
S5VLO	2	2
S6NAME	F	F
S6VHI	2	2
S6VLO	1.17	1.3
S7NAME	F	F
S7VHI	1.27	1.4
S7VLO	.8	.8

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* Schematics Circuit File *

**** Digital Gate MODEL PARAMETERS

D_LS251_1	D_LS251_4	D_LS193_1	D_LS193_2
TPLHMN	4.800000E-09	4.800000E-09	6.400000E-09
TPLHTY	12.000000E-09	12.000000E-09	16.000000E-09
TPLHMX	17.000000E-09	18.000000E-09	24.000000E-09
TPHLMN	4.000000E-09	4.000000E-09	6.000000E-09
TPHLTY	10.000000E-09	10.000000E-09	15.000000E-09
TPHLMX	17.000000E-09	18.000000E-09	24.000000E-09

D_LS86_1	D_LS86_2	D_LS86_3	D_LS08
TPLHMN	4.800000E-09	8.000000E-09	0
TPLHTY	12.000000E-09	20.000000E-09	0
TPLHMX	23.000000E-09	30.000000E-09	0
TPHLMN	0	1.200000E-09	4.000000E-09
TPHLTY	0	3.000000E-09	10.000000E-09
TPHLMX	0	5.000000E-09	17.000000E-09

D_32	D_04	D_LS123_tedge	D_LS123_edge
TPLHMN	4.000000E-09	4.800000E-09	0
TPLHTY	10.000000E-09	12.000000E-09	0
TPLHMX	15.000000E-09	22.000000E-09	0
TPHLMN	5.600000E-09	3.200000E-09	1.000000E-09
TPHLTY	14.000000E-09	8.000000E-09	1.000000E-09
TPHLMX	22.000000E-09	15.000000E-09	1.000000E-09

D_LS393_4	D0_GATE	D_LS193_6
TPLHMN	2.400000E-09	0
		19.900000E-09

TPLHTY	6.000000E-09	0	49.750000E-09
TPLHMX	6.000000E-09	0	79.600000E-09
TPHLMN	2.400000E-09	0	19.900000E-09
TPHLTY	6.000000E-09	0	49.750000E-09
TPHLMX	6.000000E-09	0	79.600000E-09

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* Schematics Circuit File *

**** Digital Tri Gate MODEL PARAMETERS

	D_LS251_3	D_LS251_6	D_LS193_4	D_LS193_5
TPLHMN	6.800000E-09	4.000000E-09	9.200000E-09	0
TPLHMX	28.000000E-09	15.000000E-09	37.000000E-09	0
TPHLMN	7.200000E-09	3.600000E-09	9.600000E-09	8.800000E-09
TPHLMX	28.000000E-09	15.000000E-09	37.000000E-09	32.000000E-09
TPZHMN	12.000000E-09	6.800000E-09	0	0
TPZHMX	45.000000E-09	27.000000E-09	0	0
TPZLMN	10.400000E-09	9.600000E-09	0	0
TPZLMX	40.000000E-09	40.000000E-09	0	0
TPLZMN	6.000000E-09	6.000000E-09	0	0
TPLZMX	25.000000E-09	25.000000E-09	0	0
TPHZMN	12.000000E-09	14.800000E-09	0	0
TPHZMX	45.000000E-09	55.000000E-09	0	0
TPLHTY	17.000000E-09	10.000000E-09	23.000000E-09	0
TPHLTY	18.000000E-09	9.000000E-09	24.000000E-09	22.000000E-09
TPZHTY	30.000000E-09	17.000000E-09	0	0
TPZLTY	26.000000E-09	24.000000E-09	0	0
TPLZTY	15.000000E-09	15.000000E-09	0	0
TPHZTY	30.000000E-09	37.000000E-09	0	0

D0_TGATE

TPLHMN	0
TPLHMX	0
TPHLMN	0
TPHLMX	0
TPZHMN	0
TPZHMX	0
TPZLMN	0
TPZLMX	0
TPLZMN	0
TPLZMX	0
TPHZMN	0
TPHZMX	0
TPLHTY	0
TPHLTY	0
TPZHTY	0
TPZLTY	0
TPLZTY	0
TPHZTY	0

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* Schematics Circuit File *

**** Digital Edge Triggered FF MODEL PARAMETERS

X_U8.D_LS123_pulse
TPCLKQLHMN 0
TPCLKQHLMN 50.000000E-06
TPPCQLHMN 0
TPPCQHLMN 0
TWCLKLMN 0
TWCLKHMN 0
TWPCLMN 0
TSUDCLKMN 0
TSUPCCLKHMN 0
THDCLKMN 0
TPCLKQLHMX 0
TPCLKQHLMX 50.005000E-06
TPPCQLHMX 0
TPPCQHLMX 0
TWCLKLMX 0
TWCLKHMX 0
TWPCLMX 0
TSUDCLKMX 0
TSUPCCLKHMX 0
THDCLKMX 0
TPCLKQLHTY 0
TPCLKQHLTY 50.002000E-06
TPPCQLHTY 0
TPPCQHLTY 0
TWCLKLTY 0
TWCLKHTY 0
TWPCLTY 0
TSUDCLKTY 0
TSUPCCLKHTY 0
THDCLKTY 0

	D_LS193_7	D_LS193_3
TPCLKQLHMN 0	9.200000E-09	1.600000E-09
TPCLKQHLMN 50.000000E-06	9.200000E-09	2.400000E-09
TPPCQLHMN 0	0	400.000000E-12
TPPCQHLMN 0	0	400.000000E-12
TWCLKLMN 0	20.000000E-09	20.000000E-09
TWCLKHMN 0	20.000000E-09	20.000000E-09
TWPCLMN 0	20.000000E-09	20.000000E-09
TSUDCLKMN 0	0	0
TSUPCCLKHMN 0	0	15.000000E-09
THDCLKMN 0	0	0
TPCLKQLHMX 0	37.000000E-09	1.000000E-09

TPCLKQHLMX	50.005000E-06	37.000000E-09	10.000000E-09
TPPCQLHMX	0	0	3.000000E-09
TPPCQHLMX	0	0	3.000000E-09
TWCLKLMX	0	20.000000E-09	20.000000E-09
TWCLKHMX	0	20.000000E-09	20.000000E-09
TWPCLMX	0	20.000000E-09	20.000000E-09
TSUDCLKMX	0	0	0
TSUPCCLKHMX	0	0	15.000000E-09
THDCLKMX	0	0	0
TPCLKQLHTY	0	23.000000E-09	4.000000E-09
TPCLKQHLTY	50.002000E-06	23.000000E-09	6.000000E-09
TPPCQLHTY	0	0	1.000000E-09
TPPCQHLTY	0	0	1.000000E-09
TWCLKLTY	0	20.000000E-09	20.000000E-09
TWCLKHTY	0	20.000000E-09	20.000000E-09
TWPCLTY	0	20.000000E-09	20.000000E-09
TSUDCLKTY	0	0	0
TSUPCCLKHTY	0	0	15.000000E-09
THDCLKTY	0	0	0

D_LS123_Outputs	D_LS393_1	D_LS393_2	D_LS393_3
TPCLKQLHMN	9.200000E-09	2.400000E-09	0
TPCLKQHLMN	12.800000E-09	2.800000E-09	0
TPPCQLHMN	11.600000E-09	0	0
TPPCQHLMN	8.000000E-09	7.200000E-09	0
TWCLKLMN	0	20.000000E-09	0
TWCLKHMN	0	20.000000E-09	0
TWPCLMN	0	20.000000E-09	0
TSUDCLKMN	0	25.000000E-09	0
TSUPCCLKHMN	0	0	0
THDCLKMN	0	0	0
TPCLKQLHMX	33.000000E-09	14.000000E-09	0
TPCLKQHLMX	45.000000E-09	14.000000E-09	0
TPPCQLHMX	39.000000E-09	0	0
TPPCQHLMX	27.000000E-09	33.000000E-09	0
TWCLKLMX	33.000000E-09	20.000000E-09	0
TWCLKHMX	0	20.000000E-09	0
TWPCLMX	0	20.000000E-09	0
TSUDCLKMX	0	25.000000E-09	0
TSUPCCLKHMX	0	0	0
THDCLKMX	0	0	0
TPCLKQLHTY	23.000000E-09	6.000000E-09	0
TPCLKQHLTY	32.000000E-09	7.000000E-09	0
TPPCQLHTY	29.000000E-09	0	0
TPPCQHLTY	20.000000E-09	18.000000E-09	0
TWCLKLTY	23.000000E-09	20.000000E-09	0
TWCLKHTY	0	20.000000E-09	0
TWPCLTY	0	20.000000E-09	0
TSUDCLKTY	0	25.000000E-09	0
TSUPCCLKHTY	0	0	0
THDCLKTY	0	0	0

**** 03/21/95 10:54:15 ***** PSpice 5.0a (Sep 1991) ***** ID# 69325 ****

* Schematics Circuit File *

**** Digital Delay Line MODEL PARAMETERS

```
X_U73.DLYMODEL X_U74.DLYMODEL X_U76.DLYMODEL D_LS123_B_dly
DLYMN 900.000000E-12 900.000000E-12 900.000000E-12 0
DLYTY 1.000000E-09 1.000000E-09 1.000000E-09 1.000000E-09
DLYMX 1.100000E-09 1.100000E-09 1.100000E-09 11.000000E-09
```

```
D_LS123_trigdly
DLYMN 1.000000E-09
DLYTY 1.000000E-09
DLYMX 1.000000E-09
```

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* Schematics Circuit File *

**** Digital IO MODEL PARAMETERS

IO_LS_ST	IO_STM	IO_LS	IO_STD
DRVL 157	0	157	104
DRVH 108	0	108	96.4
AtoD1 AtoD_LS_ST		AtoD_LS	AtoD_STD
AtoD2 AtoD_LS_ST		AtoD_LS_NX	AtoD_STD_NX
AtoD3 AtoD_LS_ST_E		AtoD_LS_E	AtoD_STD_E
AtoD4 AtoD_LS_ST_E		AtoD_LS_NXE	AtoD_STD_NXE
DtoA1 DtoA_LS	DtoA_STM	DtoA_LS	DtoA_STD
DtoA2 DtoA_LS	DtoA_STM	DtoA_LS	DtoA_STD
DtoA3 DtoA_LS	DtoA_STM	DtoA_LS	DtoA_STD
DtoA4 DtoA_LS	DtoA_STM	DtoA_LS	DtoA_STD
TSWHL1 1.995000E-09		1.995000E-09	1.373000E-09
TSWHL2 2.099000E-09		2.099000E-09	1.346000E-09
TSWHL3 2.117000E-09		2.117000E-09	1.511000E-09
TSWHL4 2.226000E-09		2.226000E-09	1.487000E-09
TSWLH1 2.730000E-09		2.730000E-09	3.382000E-09
TSWLH2 2.636000E-09		2.636000E-09	3.424000E-09
TSWLH3 2.869000E-09		2.869000E-09	3.517000E-09
TSWLH4 2.761000E-09		2.761000E-09	3.564000E-09

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* Schematics Circuit File *

**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(S3)	5.0000	(Vdd)	5.0000	(+12Vdc)	12.0000	(-12Vdc)	-12.0000
(Oscope)	2.4422	(X_U1.1)	.0030	(X_U1.8)	-1.419E-06	(X_U2.6)	-56.52E-06
(X_U2.7)	.1998	(X_U2.8)	.1998	(X_U2.9)	0.0000	(X_U3.6)	1.5010
(X_U3.7)	-12.0880	(X_U3.8)	-12.0880	(X_U3.9)	0.0000	(X_U4.6)	-27.91E-06
(X_U4.7)	.0654	(X_U4.8)	.0654	(X_U4.9)	0.0000	(\$G_DGND)	0.0000
(\$G_DPWR)	5.0000		(\$N_0092)	.0030			
(\$N_0096)	.1998		(\$N_0097)	403.3E-15			
(\$N_0099)	-.3379		(\$N_0100)	-11.9630			
(\$N_0101)	-1.3075		(\$N_0102)	-1.3076			
(\$N_0103)	943.9E-09		(\$N_0130)	-12.0000			
(\$N_0133)	10.4630		(\$N_0134)	-12.0000			
(\$N_0138)	-10.4630		(\$N_0139)	-2.6153			
(\$N_0140)	-.3379		(\$N_0141)	-11.9630			
(\$N_0142)	-2.6152		(\$N_0153)	-3.9230			
(\$N_0154)	-.3379		(\$N_0155)	-11.9630			
(\$N_0156)	-3.9229		(\$N_0167)	-5.2309			
(\$N_0168)	-.3379		(\$N_0169)	-11.9630			
(\$N_0170)	-5.2308		(\$N_0181)	-6.5389			
(\$N_0182)	-.3379		(\$N_0183)	-11.9630			
(\$N_0184)	-6.5388		(\$N_0195)	-7.8469			
(\$N_0196)	-.3379		(\$N_0197)	-11.9640			
(\$N_0198)	-7.8468		(\$N_0209)	-9.1550			
(\$N_0210)	-.3379		(\$N_0211)	-11.9640			
(\$N_0212)	-9.1549		(\$N_0230)	1.4176			
(\$N_0231)	1.9588		(\$N_0232)	1.8295			
(\$N_0237)	2.4392		(\$N_0238)	2.4422			
(\$N_0267)	2.1648		(\$N_0268)	2.0839			

(\$N_0302)	2.2919	(\$N_0303)	2.2405
(\$N_0337)	2.3702	(\$N_0338)	2.3360
(\$N_0372)	2.4180	(\$N_0373)	2.3931
(\$N_0407)	2.4465	(\$N_0408)	2.4250
(\$N_0442)	2.4625	(\$N_0443)	2.4392
(\$N_0477)	2.4696	(\$N_0517)	0.0000
(\$N_0519)	0.0000	(\$N_0520)	0.0000
(X_U1.12)	-.4877	(X_U1.13)	3.1582
(X_U1.14)	-3.1522	(X_U1.18)	3.248E-09
(X_U1.20)	6.746E-18	(X_U1.40)	-10.0000
(X_U1.60)	-12.0000	(X_U1.70)	12.0000
(X_U1.80)	-9.7454	(X_U1.90)	-9.7454
(X_U10.1)	2.4422	(X_U10.8)	-.0012
(X_U11.6)	-7.7628	(X_U11.7)	10.4690
(X_U11.8)	10.4690	(X_U11.9)	0.0000
(X_U12.6)	7.7591	(X_U12.7)	-10.5340
(X_U12.8)	-10.5340	(X_U12.9)	0.0000
(X_U16.6)	1.5030	(X_U16.7)	-12.0880
(X_U16.8)	-12.0880	(X_U16.9)	0.0000
(X_U2.10)	-.3554	(X_U2.11)	-11.6550
(X_U2.12)	-11.6550	(X_U2.53)	9.8000
(X_U2.54)	-9.8000	(X_U2.90)	307.7E-09
(X_U2.91)	25.0000	(X_U2.92)	-25.0000
(X_U2.99)	0.0000	(X_U20.6)	1.5050
(X_U20.7)	-12.0880	(X_U20.8)	-12.0880
(X_U20.9)	0.0000	(X_U23.6)	1.5071
(X_U23.7)	-12.0880	(X_U23.8)	-12.0880

(X_U23.9)	0.0000	(X_U26.6)	1.5091
(X_U26.7)	-12.0880	(X_U26.8)	-12.0880
(X_U26.9)	0.0000	(X_U29.6)	1.5111
(X_U29.7)	-12.0880	(X_U29.8)	-12.0880
(X_U29.9)	0.0000	(X_U3.10)	-.6677
(X_U3.11)	-12.0000	(X_U3.12)	-11.9200
(X_U3.13)	-.6677	(X_U3.14)	-.6956
(X_U3.53)	10.5000	(X_U3.54)	-11.3500
(X_U3.90)	-2.4894	(X_U3.91)	40.0000
(X_U3.92)	-40.0000	(X_U3.99)	0.0000
(X_U32.6)	1.5131	(X_U32.7)	-12.0880
(X_U32.8)	-12.0880	(X_U32.9)	0.0000
(X_U4.10)	-.3554	(X_U4.11)	-11.6550
(X_U4.12)	-11.6550	(X_U4.53)	9.8000
(X_U4.54)	-9.8000	(X_U4.90)	1.3076
(X_U4.91)	25.0000	(X_U4.92)	-25.0000
(X_U4.99)	0.0000	(X_U1.102)	.0030
(X_U1.103)-134.5E-12		(X_U1.131)	12.0000
(X_U1.141)	-12.0000	(X_U10.12)	1.9515
(X_U10.13)	5.5974	(X_U10.14)	-.7130
(X_U10.18)	1.686E-09	(X_U10.20)	3.502E-18
(X_U10.40)	-10.0000	(X_U10.60)	-12.0000
(X_U10.70)	12.0000	(X_U10.80)	-9.7453
(X_U10.90)	-9.7454	(X_U11.10)	-11.6010
(X_U11.11)	-11.7260	(X_U11.12)	-12.0000
(X_U11.53)	9.8000	(X_U11.54)	-9.8000
(X_U11.90)	.1098	(X_U11.91)	25.0000

(X_U11.92) -25.0000	(X_U11.99) 0.0000
(X_U12.10) -11.6010	(X_U12.11) -12.0000
(X_U12.12) -11.7260	(X_U12.53) 9.8000
(X_U12.54) -9.8000	(X_U12.90) -1.4180
(X_U12.91) 25.0000	(X_U12.92) -25.0000
(X_U12.99) 0.0000	(X_U16.10) -1.9750
(X_U16.11) -12.0000	(X_U16.12) -11.9200
(X_U16.13) -1.9750	(X_U16.14) -2.0031
(X_U16.53) 10.5000	(X_U16.54) -11.3500
(X_U16.90) -2.4894	(X_U16.91) 40.0000
(X_U16.92) -40.0000	(X_U16.99) 0.0000
(X_U20.10) -3.2824	(X_U20.11) -12.0000
(X_U20.12) -11.9190	(X_U20.13) -3.2824
(X_U20.14) -3.3107	(X_U20.53) 10.5000
(X_U20.54) -11.3500	(X_U20.90) -2.4895
(X_U20.91) 40.0000	(X_U20.92) -40.0000
(X_U20.99) 0.0000	(X_U23.10) -4.5899
(X_U23.11) -12.0000	(X_U23.12) -11.9190
(X_U23.13) -4.5899	(X_U23.14) -4.6184
(X_U23.53) 10.5000	(X_U23.54) -11.3500
(X_U23.90) -2.4895	(X_U23.91) 40.0000
(X_U23.92) -40.0000	(X_U23.99) 0.0000
(X_U26.10) -5.8975	(X_U26.11) -12.0000
(X_U26.12) -11.9180	(X_U26.13) -5.8975
(X_U26.14) -5.9262	(X_U26.53) 10.5000
(X_U26.54) -11.3500	(X_U26.90) -2.4895
(X_U26.91) 40.0000	(X_U26.92) -40.0000

(X_U26.99) 0.0000	(X_U29.10) -7.2052
(X_U29.11) -12.0000	(X_U29.12) -11.9180
(X_U29.13) -7.2052	(X_U29.14) -7.2341
(X_U29.53) 10.5000	(X_U29.54) -11.3500
(X_U29.90) -2.4895	(X_U29.91) 40.0000
(X_U29.92) -40.0000	(X_U29.99) 0.0000
(X_U32.10) -8.5130	(X_U32.11) -12.0000
(X_U32.12) -11.9170	(X_U32.13) -8.5130
(X_U32.14) -8.5421	(X_U32.53) 10.5000
(X_U32.54) -11.3500	(X_U32.90) -2.4896
(X_U32.91) 40.0000	(X_U32.92) -40.0000
(X_U32.99) 0.0000	(X_U10.102) 2.4422
(X_U10.103) 2.4392	(X_U10.131) 12.0000
(X_U10.141) -12.0000	(Photo_Detector) 0.0000

DGTL NODE : STATE DGTL NODE : STATE DGTL NODE : STATE DGTL NODE : STATE

(.) : 1	(0A) : Z	(0B) : Z	(0C) : Z
(0D) : Z	(0E) : Z	(0F) : Z	(0G) : Z
(0H) : Z	(1A) : X	(1B) : X	(1C) : X
(1D) : X	(1E) : X	(1F) : X	(1G) : X
(1H) : X	(2A) : X	(2B) : X	(2C) : X
(2D) : X	(2E) : X	(2F) : X	(2G) : X
(2H) : X	(3A) : X	(3B) : X	(3C) : X
(3D) : X	(3E) : X	(3F) : X	(3G) : X
(3H) : X	(4A) : X	(4B) : X	(4C) : X
(4D) : X	(4E) : X	(4F) : X	(4G) : X
(4H) : X	(5A) : X	(5B) : X	(5C) : X

(5D) : X (5E) : X (5F) : X (5G) : X
 (5H) : X (6A) : X (6B) : X (6C) : X
 (6D) : X (6E) : X (6F) : X (6G) : X
 (6H) : X (7A) : X (7B) : X (7C) : X
 (7D) : X (7E) : X (7F) : X (7G) : X
 (7H) : X (MC) : 0 (PC) : 0 (S0) : 0
 (S1) : 0 (S2) : 0 (SC) : 0 (\$D_X) : X
 (\$D_HI) : 1 (\$D_LO) : 0 (\$D_NC) : Z (CTR-0) : 0
 (CTR-1) : 0 (CTR-2) : 0 (CTR-3) : 0 (CTR-4) : 0
 (CTR-5) : 0 (CTR-6) : 0 (CTR-7) : 0 (muxen) : 1
 (reset) : 0 (0\$AtoD) : 0 (X_U5.C) : 1 (X_U5.D) : 1
 (\$N_0110) : 1 (\$N_0113) : 0 (\$N_0124) : 0 (\$N_0147) : 0
 (\$N_0161) : 0 (\$N_0175) : 0 (\$N_0189) : 0 (\$N_0203) : 0
 (\$N_0217) : 0 (\$N_0224) : 0 (\$N_0271) : X (\$N_0306) : X
 (\$N_0341) : X (\$N_0376) : X (\$N_0411) : X (\$N_0446) : X
 (\$N_0480) : X (S3\$AtoD) : 1 (S3\$DtoA) : Z (X_U17.C) : 0
 (X_U17.D) : 1 (X_U19.E) : X (X_U19.F) : X (X_U19.G) : 0
 (X_U19.J) : 0 (X_U19.K) : 0 (X_U19.L) : 0 (X_U19.P) : 0
 (X_U19.Q) : 0 (X_U19.R) : 0 (X_U21.C) : 0 (X_U21.D) : 1
 (X_U24.C) : 0 (X_U24.D) : 1 (X_U27.C) : 0 (X_U27.D) : 1
 (X_U30.C) : 0 (X_U30.D) : 1 (X_U33.C) : 0 (X_U33.D) : 1
 (X_U35.C) : 0 (X_U35.D) : 1 (X_U41.E) : X (X_U41.F) : X
 (X_U41.G) : 0 (X_U41.J) : 0 (X_U41.K) : 0 (X_U41.L) : 0
 (X_U41.P) : 0 (X_U41.Q) : 0 (X_U41.R) : 0 (X_U46.E) : X
 (X_U46.F) : X (X_U46.G) : 0 (X_U46.J) : 0 (X_U46.K) : 0
 (X_U46.L) : 0 (X_U46.P) : 0 (X_U46.Q) : 0 (X_U46.R) : 0
 (X_U51.E) : X (X_U51.F) : X (X_U51.G) : 0 (X_U51.J) : 0

(X_U51.K) : 0 (X_U51.L) : 0 (X_U51.P) : 0 (X_U51.Q) : 0
(X_U51.R) : 0 (X_U56.E) : X (X_U56.F) : X (X_U56.G) : 0
(X_U56.J) : 0 (X_U56.K) : 0 (X_U56.L) : 0 (X_U56.P) : 0
(X_U56.Q) : 0 (X_U56.R) : 0 (X_U61.E) : X (X_U61.F) : X
(X_U61.G) : 0 (X_U61.J) : 0 (X_U61.K) : 0 (X_U61.L) : 0
(X_U61.P) : 0 (X_U61.Q) : 0 (X_U61.R) : 0 (X_U66.E) : X
(X_U66.F) : X (X_U66.G) : 0 (X_U66.J) : 0 (X_U66.K) : 0
(X_U66.L) : 0 (X_U66.P) : 0 (X_U66.Q) : 0 (X_U66.R) : 0
(X_U71.E) : X (X_U71.F) : X (X_U71.G) : 0 (X_U71.J) : 0
(X_U71.K) : 0 (X_U71.L) : 0 (X_U71.P) : 0 (X_U71.Q) : 0
(X_U71.R) : 0 (S3\$AtoD2) : 1 (S3\$DtoA2) : 0 (Vdd\$AtoD) : 1
(X_U75.AK) : 1 (X_U75.AN) : 0 (X_U75.AX) : X (X_U75.BK) : 1
(X_U75.BN) : 0 (X_U75.BX) : X (X_U75.CA) : 0 (X_U75.CB) : 0
(X_U75.CC) : 0 (X_U75.CD) : 0 (X_U75.CK) : 1 (X_U75.CN) : 0
(X_U75.CX) : X (X_U75.DK) : 1 (X_U75.DN) : 0 (X_U75.DX) : X
(X_U75.PA) : 1 (X_U75.PB) : 1 (X_U75.PC) : 1 (X_U75.PD) : 1
(X_U75.Q0) : 0 (X_U75.Q1) : 0 (X_U75.Q2) : 0 (X_U75.Q3) : 0
(X_U75.ABF) : X (X_U75.BBF) : X (X_U75.CBF) : X (X_U75.CLA) : 1
(X_U75.CLB) : 1 (X_U75.CLC) : 1 (X_U75.CLD) : 1 (X_U75.DBF) : X
(X_U75.UPB) : 1 (X_U8.ABar) : 1 (X_U19.JBAR) : 1 (X_U19.KBAR) : 1
(X_U19.LBAR) : 1 (X_U19.PBAR) : 1 (X_U19.QBAR) : 1 (X_U19.RBAR) : 1
(X_U41.JBAR) : 1 (X_U41.KBAR) : 1 (X_U41.LBAR) : 1 (X_U41.PBAR) : 1
(X_U41.QBAR) : 1 (X_U41.RBAR) : 1 (X_U46.JBAR) : 1 (X_U46.KBAR) : 1
(X_U46.LBAR) : 1 (X_U46.PBAR) : 1 (X_U46.QBAR) : 1 (X_U46.RBAR) : 1
(X_U5.A_BUF) : 1 (X_U5.B_BUF) : 0 (X_U51.JBAR) : 1 (X_U51.KBAR) : 1
(X_U51.LBAR) : 1 (X_U51.PBAR) : 1 (X_U51.QBAR) : 1 (X_U51.RBAR) : 1
(X_U56.JBAR) : 1 (X_U56.KBAR) : 1 (X_U56.LBAR) : 1 (X_U56.PBAR) : 1

(X_U56.QBAR) : 1 (X_U56.RBAR) : 1 (X_U61.JBAR) : 1 (X_U61.KBAR) : 1
 (X_U61.LBAR) : 1 (X_U61.PBAR) : 1 (X_U61.QBAR) : 1 (X_U61.RBAR) : 1
 (X_U66.JBAR) : 1 (X_U66.KBAR) : 1 (X_U66.LBAR) : 1 (X_U66.PBAR) : 1
 (X_U66.QBAR) : 1 (X_U66.RBAR) : 1 (X_U71.JBAR) : 1 (X_U71.KBAR) : 1
 (X_U71.LBAR) : 1 (X_U71.PBAR) : 1 (X_U71.QBAR) : 1 (X_U71.RBAR) : 1
 (X_U72.ABar) : 1 (X_U75.CLKA) : 1 (X_U75.CLKB) : 0 (X_U75.CLKC) : 0
 (X_U75.CLKD) : 0 (X_U75.CLRA) : 0 (X_U75.CLRB) : 0 (X_U75.CLRC) : 0
 (X_U75.CLRD) : 0 (X_U75.LOAD) : 0 (X_U75.PREA) : 1 (X_U75.PREB) : 1
 (X_U75.PREC) : 1 (X_U75.PRED) : 1 (X_U8.B_dly) : 0 (X_U8.Clear) : 0
 (X_U8.Reset) : X (X_U8.trigx) : 0 (X_U17.A_BUF) : 0 (X_U17.B_BUF) : 0
 (X_U19.A_BUF) : 0 (X_U19.B_BUF) : 0 (X_U19.C_BUF) : 0 (X_U21.A_BUF) : 0
 (X_U21.B_BUF) : 0 (X_U24.A_BUF) : 0 (X_U24.B_BUF) : 0 (X_U27.A_BUF) : 0
 (X_U27.B_BUF) : 0 (X_U30.A_BUF) : 0 (X_U30.B_BUF) : 0 (X_U33.A_BUF) : 0
 (X_U33.B_BUF) : 0 (X_U35.A_BUF) : 0 (X_U35.B_BUF) : 0 (X_U41.A_BUF) : 0
 (X_U41.B_BUF) : 0 (X_U41.C_BUF) : 0 (X_U46.A_BUF) : 0 (X_U46.B_BUF) : 0
 (X_U46.C_BUF) : 0 (X_U51.A_BUF) : 0 (X_U51.B_BUF) : 0 (X_U51.C_BUF) : 0
 (X_U56.A_BUF) : 0 (X_U56.B_BUF) : 0 (X_U56.C_BUF) : 0 (X_U61.A_BUF) : 0
 (X_U61.B_BUF) : 0 (X_U61.C_BUF) : 0 (X_U66.A_BUF) : 0 (X_U66.B_BUF) : 0
 (X_U66.C_BUF) : 0 (X_U71.A_BUF) : 0 (X_U71.B_BUF) : 0 (X_U71.C_BUF) : 0
 (X_U72.B_dly) : 0 (X_U72.Clear) : 0 (X_U72.Reset) : X (X_U72.trigx) : 0
 (X_U75.CLRBD) : 0 (X_U75.CLRDE) : 1 (X_U75.DOWNB) : 0 (X_U75.LOADB) : 1
 (X_U75.Q0BAR) : 1 (X_U75.Q1BAR) : 1 (X_U75.Q2BAR) : 1 (X_U75.Q3BAR) : 1
 (X_U75.X1.AB) : X (X_U75.X1.BB) : X (X_U75.X1.CB) : X (X_U75.X1.DB) : X
 (X_U8.reset0) : 1 (X_U8.Trig_0) : 1 (\$N_0099\$AtoD) : 0
 (\$N_0140\$AtoD) : 0 (\$N_0154\$AtoD) : 0
 (\$N_0168\$AtoD) : 0 (\$N_0182\$AtoD) : 0
 (\$N_0196\$AtoD) : 0 (\$N_0210\$AtoD) : 0

(\$N_0231\$DtoA) : Z	(\$N_0267\$DtoA) : Z
(\$N_0302\$DtoA) : Z	(\$N_0337\$DtoA) : Z
(\$N_0372\$DtoA) : Z	(\$N_0407\$DtoA) : Z
(\$N_0442\$DtoA) : Z	(\$N_0477\$DtoA) : Z
(\$N_0517\$AtoD) : 0	(\$N_0519\$AtoD) : 0
(\$N_0520\$AtoD) : 0	(X_U19.D0_BUF) : X
(X_U19.D1_BUF) : X	(X_U19.D2_BUF) : X
(X_U19.D3_BUF) : X	(X_U19.D4_BUF) : X
(X_U19.D5_BUF) : X	(X_U19.D6_BUF) : X
(X_U19.D7_BUF) : X	(X_U37.CLRBAR) : 1
(X_U37.QA_BUF) : X	(X_U37.QB_BUF) : X
(X_U37.QC_BUF) : X	(X_U37.QD_BUF) : X
(X_U38.CLRBAR) : 1	(X_U38.QA_BUF) : X
(X_U38.QB_BUF) : X	(X_U38.QC_BUF) : X
(X_U38.QD_BUF) : X	(X_U41.D0_BUF) : X
(X_U41.D1_BUF) : X	(X_U41.D2_BUF) : X
(X_U41.D3_BUF) : X	(X_U41.D4_BUF) : X
(X_U41.D5_BUF) : X	(X_U41.D6_BUF) : X
(X_U41.D7_BUF) : X	(X_U42.CLRBAR) : 1
(X_U42.QA_BUF) : X	(X_U42.QB_BUF) : X
(X_U42.QC_BUF) : X	(X_U42.QD_BUF) : X
(X_U43.CLRBAR) : 1	(X_U43.QA_BUF) : X
(X_U43.QB_BUF) : X	(X_U43.QC_BUF) : X
(X_U43.QD_BUF) : X	(X_U46.D0_BUF) : X
(X_U46.D1_BUF) : X	(X_U46.D2_BUF) : X
(X_U46.D3_BUF) : X	(X_U46.D4_BUF) : X
(X_U46.D5_BUF) : X	(X_U46.D6_BUF) : X

(X_U46.D7_BUF) : X	(X_U47.CLRBAR) : 1
(X_U47.QA_BUF) : X	(X_U47.QB_BUF) : X
(X_U47.QC_BUF) : X	(X_U47.QD_BUF) : X
(X_U48.CLRBAR) : 1	(X_U48.QA_BUF) : X
(X_U48.QB_BUF) : X	(X_U48.QC_BUF) : X
(X_U48.QD_BUF) : X	(X_U51.D0_BUF) : X
(X_U51.D1_BUF) : X	(X_U51.D2_BUF) : X
(X_U51.D3_BUF) : X	(X_U51.D4_BUF) : X
(X_U51.D5_BUF) : X	(X_U51.D6_BUF) : X
(X_U51.D7_BUF) : X	(X_U52.CLRBAR) : 1
(X_U52.QA_BUF) : X	(X_U52.QB_BUF) : X
(X_U52.QC_BUF) : X	(X_U52.QD_BUF) : X
(X_U53.CLRBAR) : 1	(X_U53.QA_BUF) : X
(X_U53.QB_BUF) : X	(X_U53.QC_BUF) : X
(X_U53.QD_BUF) : X	(X_U56.D0_BUF) : X
(X_U56.D1_BUF) : X	(X_U56.D2_BUF) : X
(X_U56.D3_BUF) : X	(X_U56.D4_BUF) : X
(X_U56.D5_BUF) : X	(X_U56.D6_BUF) : X
(X_U56.D7_BUF) : X	(X_U57.CLRBAR) : 1
(X_U57.QA_BUF) : X	(X_U57.QB_BUF) : X
(X_U57.QC_BUF) : X	(X_U57.QD_BUF) : X
(X_U58.CLRBAR) : 1	(X_U58.QA_BUF) : X
(X_U58.QB_BUF) : X	(X_U58.QC_BUF) : X
(X_U58.QD_BUF) : X	(X_U61.D0_BUF) : X
(X_U61.D1_BUF) : X	(X_U61.D2_BUF) : X
(X_U61.D3_BUF) : X	(X_U61.D4_BUF) : X
(X_U61.D5_BUF) : X	(X_U61.D6_BUF) : X

(X_U61.D7_BUF) : X	(X_U62.CLRBAR) : 1
(X_U62.QA_BUF) : X	(X_U62.QB_BUF) : X
(X_U62.QC_BUF) : X	(X_U62.QD_BUF) : X
(X_U63.CLRBAR) : 1	(X_U63.QA_BUF) : X
(X_U63.QB_BUF) : X	(X_U63.QC_BUF) : X
(X_U63.QD_BUF) : X	(X_U66.D0_BUF) : X
(X_U66.D1_BUF) : X	(X_U66.D2_BUF) : X
(X_U66.D3_BUF) : X	(X_U66.D4_BUF) : X
(X_U66.D5_BUF) : X	(X_U66.D6_BUF) : X
(X_U66.D7_BUF) : X	(X_U67.CLRBAR) : 1
(X_U67.QA_BUF) : X	(X_U67.QB_BUF) : X
(X_U67.QC_BUF) : X	(X_U67.QD_BUF) : X
(X_U68.CLRBAR) : 1	(X_U68.QA_BUF) : X
(X_U68.QB_BUF) : X	(X_U68.QC_BUF) : X
(X_U68.QD_BUF) : X	(X_U71.D0_BUF) : X
(X_U71.D1_BUF) : X	(X_U71.D2_BUF) : X
(X_U71.D3_BUF) : X	(X_U71.D4_BUF) : X
(X_U71.D5_BUF) : X	(X_U71.D6_BUF) : X
(X_U71.D7_BUF) : X	(X_U72.reset0) : 1
(X_U72.Trig_0) : 1	(X_U75.CLRBAR) : 0
(X_U8.trigdly) : 0	(X_U8.Trigger) : 0
(\$N_0099\$AtoD2) : 0	(\$N_0140\$AtoD2) : 0
(\$N_0154\$AtoD2) : 0	(\$N_0168\$AtoD2) : 0
(\$N_0182\$AtoD2) : 0	(\$N_0196\$AtoD2) : 0
(\$N_0210\$AtoD2) : 0	(X_U72.trigdly) : 0
(X_U72.Trigger) : 0	(X_U8.Trig_Bar) : 1
(X_U72.Trig_Bar) : 1	(X_U8.reset_bar) : X

(X_U8.Trig0_Bar) : 0	(X_U8.trigx_bar) : 1
(X_U72.reset_bar) : X	(X_U72.Trig0_Bar) : 0
(X_U72.trigx_bar) : 1	(X_U8.TrigPreset) : 1
(X_U8.trigx_fall) : 0	(X_U72.TrigPreset) : 1
(X_U72.trigx_fall) : 0	(X_U8.trigx_barbar) : 0
(X_U72.trigx_barbar) : 0	

VOLTAGE SOURCE CURRENTS
NAME CURRENT

v_V1	-2.574E-04
V_V5	0.000E+00
V_V6	0.000E+00
V_V7	0.000E+00
V_V8	-1.689E-01
v_V2	3.533E-02
v_V3	-3.567E-02
v_V4	-7.916E-05
V_V10	-2.028E-10
X_U1.vcm2	4.800E-04
X_U1.vc	8.842E-12
X_U1.ve	6.949E-12
X_U2.vb	-5.652E-10
X_U2.vc	9.601E-12
X_U2.ve	1.000E-11
X_U2.vlim	3.077E-10
X_U2.vlp	-2.500E-11
X_U2.vln	-2.500E-11
X_U3.vb	1.501E-05
X_U3.vc	2.246E-11
X_U3.ve	-1.590E-05
X_U3.vlim	-2.489E-03
X_U3.vlp	-4.249E-11
X_U3.vln	-3.751E-11
X_U4.vb	-2.791E-10
X_U4.vc	9.801E-12
X_U4.ve	9.801E-12
X_U4.vlim	1.308E-03
X_U4.vlp	-2.369E-11
X_U4.vln	-2.631E-11
X_U11.vb	-7.763E-05
X_U11.vc	-1.098E-04
X_U11.ve	2.026E-11
X_U11.vlim	1.098E-04
X_U11.vlp	-2.489E-11
X_U11.vln	-2.511E-11
X_U12.vb	7.759E-05

X_U12.vc 2.026E-11
X_U12.ve -1.097E-04
X_U12.vlim -1.418E-03
X_U12.vlp -2.642E-11
X_U12.vln -2.358E-11
X_U16.vb 1.503E-05
X_U16.vc 2.246E-11
X_U16.ve -1.592E-05
X_U16.vlim -2.489E-03
X_U16.vlp -4.249E-11
X_U16.vln -3.751E-11
X_U20.vb 1.505E-05
X_U20.vc 2.246E-11
X_U20.ve -1.594E-05
X_U20.vlim -2.489E-03
X_U20.vlp -4.249E-11
X_U20.vln -3.751E-11
X_U23.vb 1.507E-05
X_U23.vc 2.246E-11
X_U23.ve -1.597E-05
X_U23.vlim -2.489E-03
X_U23.vlp -4.249E-11
X_U23.vln -3.751E-11
X_U26.vb 1.509E-05
X_U26.vc 2.246E-11
X_U26.ve -1.599E-05
X_U26.vlim -2.490E-03
X_U26.vlp -4.249E-11
X_U26.vln -3.751E-11
X_U29.vb 1.511E-05
X_U29.vc 2.246E-11
X_U29.ve -1.601E-05
X_U29.vlim -2.490E-03
X_U29.vlp -4.249E-11
X_U29.vln -3.751E-11
X_U32.vb 1.513E-05
X_U32.vc 2.246E-11
X_U32.ve -1.603E-05
X_U32.vlim -2.490E-03
X_U32.vlp -4.249E-11
X_U32.vln -3.751E-11
X_U10.vcm2 4.800E-04
X_U10.vc 6.403E-12
X_U10.ve 1.129E-11
X\$DIGIFPWR.VDPWR -1.121E-04
X\$DIGIFPWR.VDGND 1.689E-01

TOTAL POWER DISSIPATION 1.70E+00 WATTS

I/O ERROR -- On file DIG14101.TMP. The disk is probably full

PSPICE ABORTING**** 03/21/95 10:54:15 ***** PSpice 5.0a (Sep 1991) ***** ID# 69325 ****

* Schematics Circuit File *

***** JOB STATISTICS SUMMARY

NUNODS NCNODS NUMNOD NUMEL DIODES BJTS JFETS MFETS GASFETS

63 255 306 811 85 14 12 0 0

NDIGITAL NSTOP NTTAR NTTBR NTTOV IFILL IOPS PERSPA

280 413 1626 3035 1433 1409 14506 98.221

NUMTTP NUMRTP NUMNIT DIGTP DIGEVT DIGEVL MEMUSE

20123 10 60402 256 2008 1454 621656

SECONDS ITERATIONS

MATRIX SOLUTION 2120.78 4

MATRIX LOAD 785.55

DIGITAL SIMULATION .23

READIN 5.03

SETUP .13

DC SWEEP 0.00 0

BIAS POINT 19.93 264

AC and NOISE 0.00 0

TRANSIENT ANALYSIS 3365.00 60402

OUTPUT 0.00

TOTAL JOB TIME 3370.23

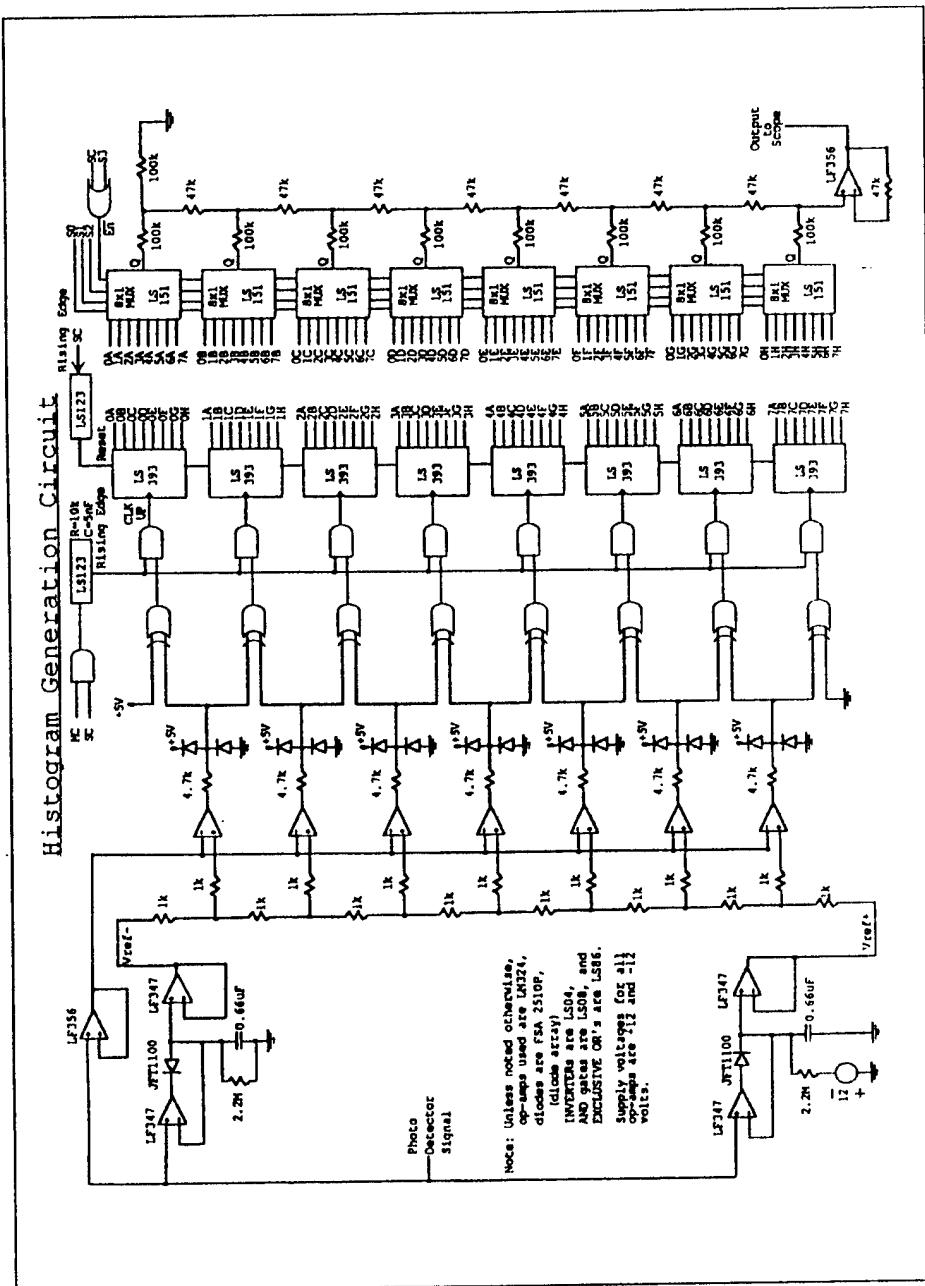


Figure 22. Original Histogram Generation Circuit

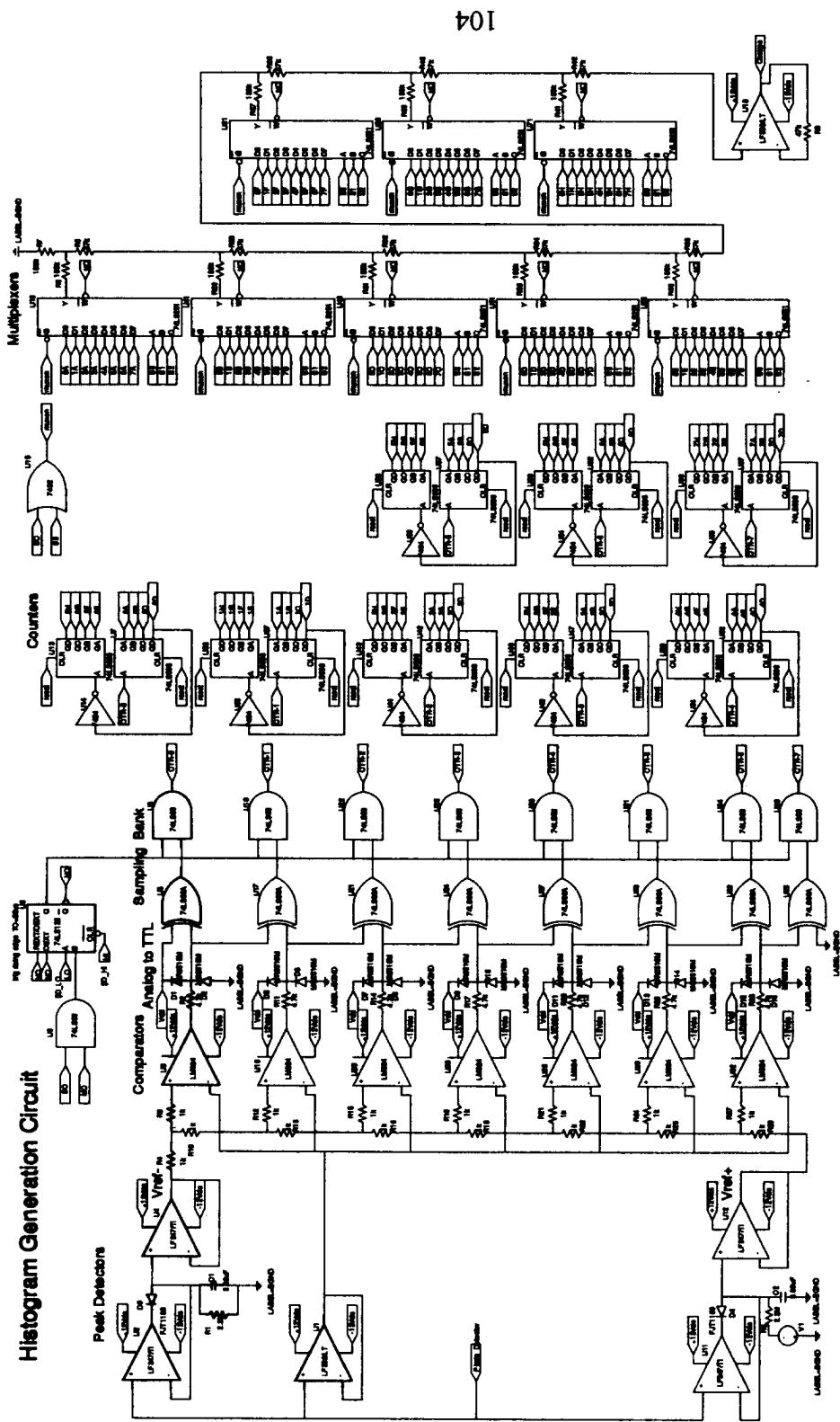


Figure 23. Pspice Histogram Generation Circuit

Timing Circuit

Note: The last pulse of N pulses is extremely narrow due to timing of inputs to LS02, and it may not be seen on the scope.

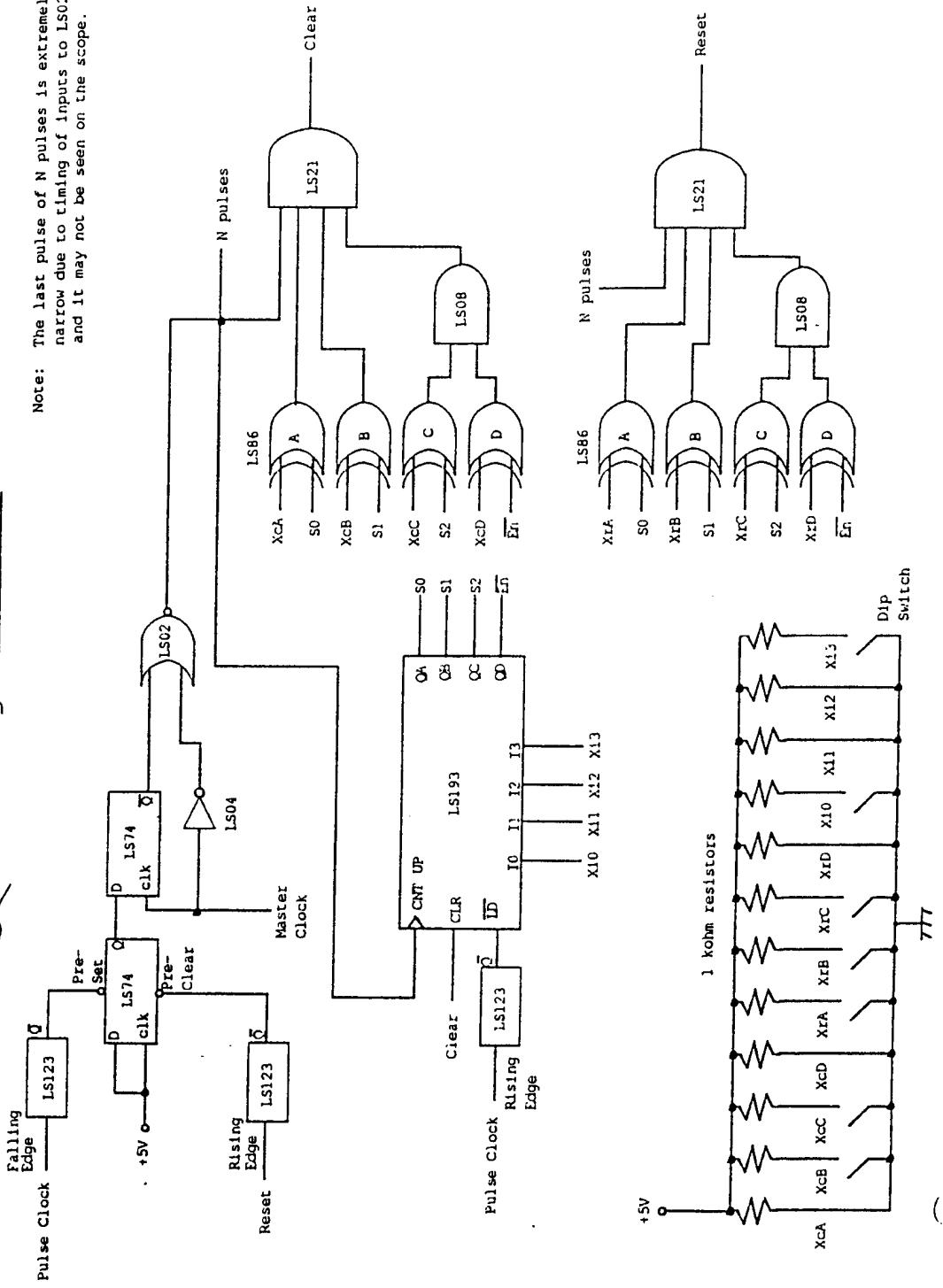
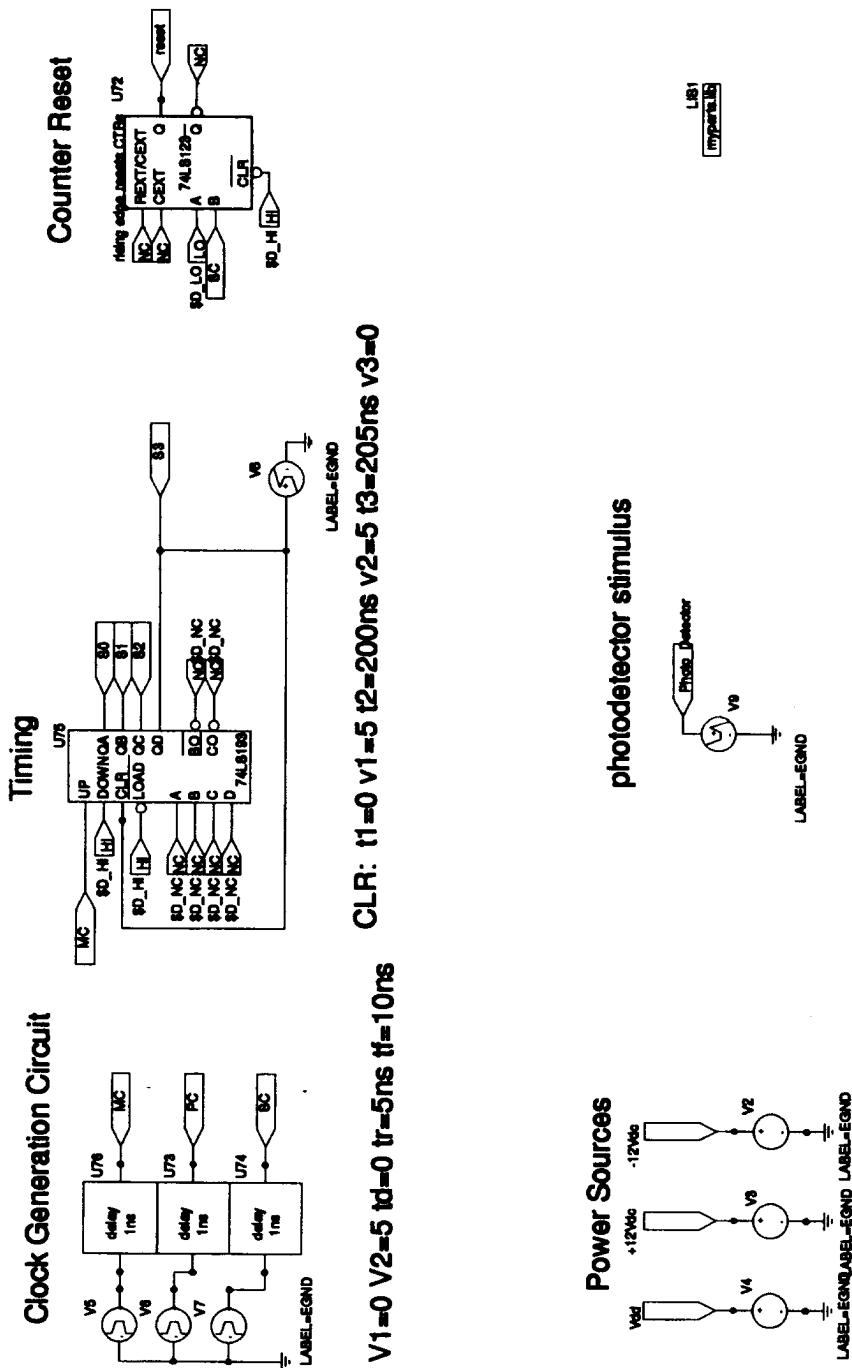


Figure 24. Original Timing Circuit

Figure 25. Spice Timing Circuit



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